Modelling electromagnetic field coupling from an ESD gun to an IC

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Abstract— **IC designers require fast and accurate methods of simulating immunity of ICs to ESD events to adequately predict and analyze ESD issues. The common method of predicting electromagnetic field coupling from an ESD gun to an IC, however, requires substantial simulation time and does not typically account for the full IC layout. Here we propose an efficient methodology for calculating the electromagnetic field coupling from an ESD gun to an IC while fully considering the non-linear circuit elements in the IC core. Voltages and currents within the IC are found by merging full-wave simulations of an ESD gun with a SPICE model of the IC and the coupled electromagnetic energy. The capability of the proposed method was verified through experiments on a pseudo- integrated circuit structure. Results show the promise of the method. This hybrid modelling method can significantly accelerate simulation time compared with traditional full-wave modelling techniques and can allow the designer to better explore the variation in coupling that occurs with small changes in the test setup, such as the position and orientation of the gun and IC.**

I. Introduction

Electrostatic discharge (ESD) can significantly damage Integrated Circuits (ICs). The potential of an IC to be damaged is accessed through a variety of tests. In one test, illustrated in Fig. 1, an ESD generator is placed a short distance from the IC and discharged to the return plane [1]. ESD failures occur largely due to electric or magnetic field coupling from the ESD gun to the IC. This test is sensitive to the relative positions of the IC and ESD gun, the rotation of the gun or IC, the length and termination of the grounding strap, as well as other factors. These and other factors can cause a great deal of variation in test results and test repeatability. Models are needed that not only predict the field coupling from the ESD gun to the IC, but that are fast enough that these variations can be explored. Accurate models can allow the IC designer to better predict the immunity of their ICs and to better understand the causes of susceptibility problems when they occur.

In order to build a good model of the electromagnetic field coupling and to estimate the response of the IC precisely, some essential elements are required: a complete model of the ESD generator, a detailed model of the IC package, and a relatively complete model of the circuit inside the IC (including non-linear components like ESD protection circuitry). These elements allow accurate prediction of voltage and currents within the IC and the potential damage they may cause.

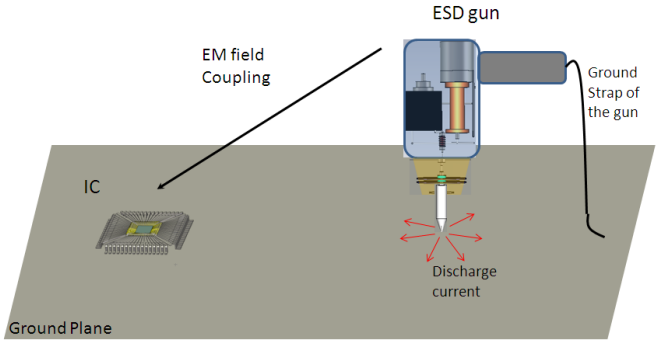

Fig 1: Electromagnetic coupling during the standard ESD gun test

A common approach of predicting the currents and voltages in the IC is to use a full-wave model of the ESD gun and IC package [2][3]. Modelling the IC package requires a relatively fine mesh compared to modelling the relatively large ESD gun, resulting in a very large mesh and very long simulation times. For example, simulation of the ESD gun and the 1.5 cm by 1.5 cm microcontroller package over 20 nS in [2] required nearly 50 hours to complete. This simulation time might be acceptable if only one simulation was needed, but accounting for variations in the setup, like the position of the IC and gun, potentially requires the simulation of many IC/gun configurations.

Another disadvantage of a pure full wave simulation approach is that most commercial software only supports simple linear circuit elements, like resistors, inductors, and capacitors. Dealing with very complicated IC layouts that include non-linear circuitry is challenging [4][5].

In this paper, a fast and accurate method is proposed for predicting the IC's response to electromagnetic field coupling from an ESD gun during a discharge event. The method separates the full-wave modelling of the fields generated by the gun from the simulation of the response of the IC to the coupled fields. This approach has three advantages over a purely full wave technique:

1. It requires much less computation time because the big ESD model and the relatively small IC package model are simulated separately. The full-wave solver only needs to calculate the field generated from the gun, without the presence of the IC package.

2. It accounts for the complete non-linear IC circuit, by performing the simulation of the IC in SPICE.
3. It allows the designer to rapidly change the relative orientation of the IC and gun without re-simulating the fields generated by the gun. Only the currents and voltages caused by the fields in the SPICE model need to be changed.

The proposed methodology consists of three steps: estimation of the electromagnetic fields generated by the gun; development of an equivalent SPICE model of the IC package (including active sources which represent the electromagnetic field coupling); and simulation of the IC package and core model to predict voltage and currents in the die generated by the ESD event. The following sections explain the methodology and show the potential of the approach through experimentation.

II. Methodology

As depicted in Fig 2, the proposed method first estimates the electric and magnetic fields generated by an ESD gun during a discharge event. These simulations are performed in a full-wave solver and include only the gun and return plane – not the IC. Next, a SPICE model of the IC package is developed that includes self and mutual inductances associated with the package as well as current and voltage sources that represent electric and magnetic field coupling from the gun to the IC package. Finally, the package model is combined with a SPICE model of the IC power delivery network and I/O to predict the voltage and currents that appear on-die. Each step explained below.

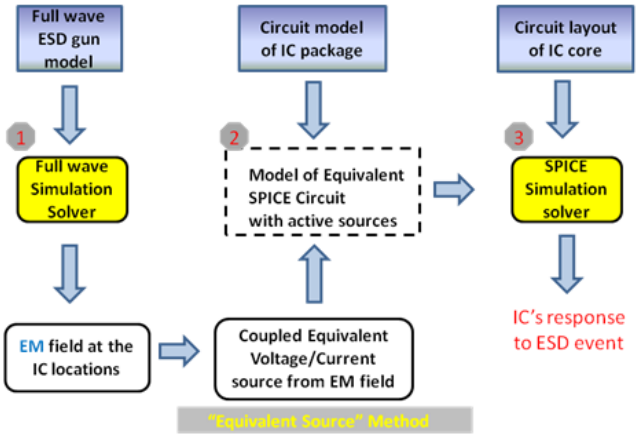

Fig 2: Proposed simulation methodology

1. *Calculate fields generated by the ESD gun*

During this step, the complete ESD gun is represented in the 3D environment and the IC package model is not present. The IC can be removed from the model since the presence of the IC has little impact on the voltage and currents in the gun. This assumption has been tested in simulations and proven to be correct. Without the IC package, the size of the mesh can be significantly reduced.

As shown in Fig 3, the results of the simulation are electric and magnetic field components (specifically Ez, Hx and Hy) in the region of the IC. These field components are used to predict voltage and current sources representing electric and magnetic field coupling to the package. In Fig. 3, the locations of the recorded fields exactly correspond to positions of IC pins. The green arrows represent the Ez field components, while the blue arrows represent the recorded Hx and Hy field components. In general, many field components may be recorded to allow the position of the IC to be "moved" relative to the gun.

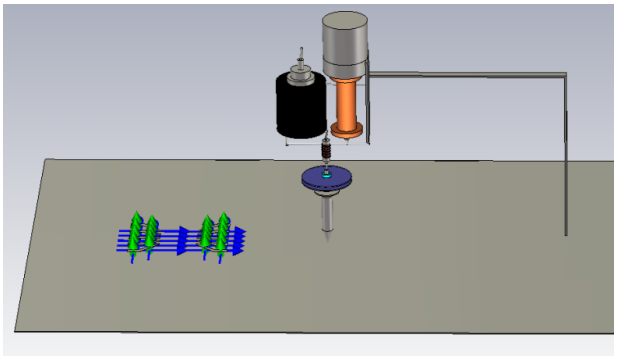

Fig 3: Calculated electric and magnetic fields from a full wave model of the ESD gun.

2. *Build SPICE model of IC package and field coupling.*

The SPICE model of the package contains two parts: a passive portion representing the parasitics of the IC package, and an active portion consisting of the equivalent current and voltage sources representing the electromagnetic field coupling. The passive portions of the model are determined from the geometry of the IC package. At low frequencies, simple lumped elements (R, L and C) can be used. At high frequencies, a distributed model is required.

There are two approaches to obtain the passive package model: a) extract the self and mutual inductance and capacitance of pins from simulation; or b) extract these parasitics from S-parameter measurements. To extract package parameters from simulation, the package geometry is modelled in detail and an inductance/capacitance matrix is calculated. The mutual inductance and capacitance between each pin of interest and its neighbouring pins is essential. Methods of extracting similar parameters from measurement will be introduced in section III.

An example of a simple model of an IC pin and coupling to neighbouring pins is shown in Fig 4 and Fig 5. To illustrate the concept, Fig 5 shows the mutual coupling between two pins. Each pin is modelled as a separate loop, consisting of a parasitic inductance, a parasitic capacitance, termination impedance, a voltage source, representing magnetic field coupling, a current source, representing electric field coupling, and mutual inductance and capacitance to neighbouring pins. Mutual inductances and capacitances are highlighted using yellow and blue circles. Here, coupling is only shown between two pins. In a real IC, more pins should be included in the model. Experiments performed in our lab suggest that coupling to at least 5 to 6 neighbouring pins should be included for a PLCC package.

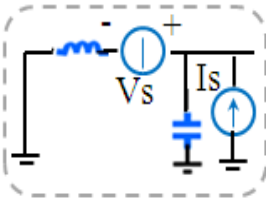

Fig 4: Model of a single pin

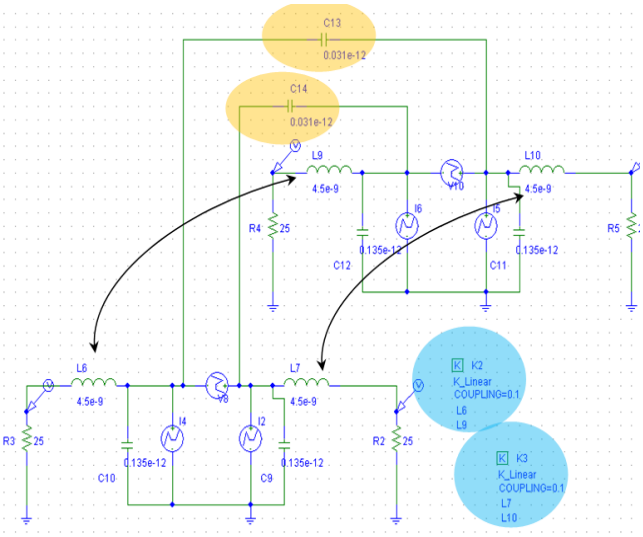

Fig 5: Simplified circuit model of coupling between two IC pins

The "active" voltage and current sources at each pin are calculated from the electric and magnetic fields generated by the ESD gun. Fig 6 shows the geometry of an IC pins and the generated magnetic field passing through the loop induces a voltage drop across the loop. This voltage is given by

$$V_s = -\iint \left(\frac{dH_n}{dt}\mu\right) dA_{eff} \qquad (1)$$

where dA_{eff} is the differential component of the loop area, H_n is the magnetic field component normal to the loop area, μ is the free-space permeability, and t is time. Simulations show that, for a 2 cm by 2 cm package whose center is 5 cm from the ESD gun as in [1], there is no drastic variation of the field within a single pin loop area so that the voltage source is approximately given by

$$V_s \approx -\frac{dH_n}{dt}\mu \cdot A_{eff} \qquad (2)$$

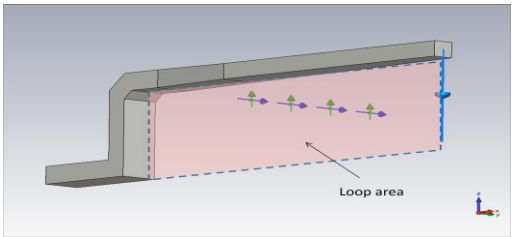

Fig 6: H-field generating the voltage source

Electric field coupling is calculated in a similar manner. The electric field is shown in Fig 7. Due to the low height of a typical IC, only the field incident on the horizontal portion of the pin (i.e. the Ez field) is important. The horizontal fields incident on the vertical portion of the pin can be neglected. The current source in Fig 4 is calculated as

$$I_s = -\iint \left(\frac{dE_Z}{dt}\varepsilon\right) dS \qquad (3)$$

where E_Z is the vertical electrical field, ε is permittivity, and S is the differential surface area of the pin. As before, since the field varies slowly over the IC, the current may be approximated as

$$I_s = -\frac{dE_Z}{dt}\varepsilon \cdot S \qquad (4)$$

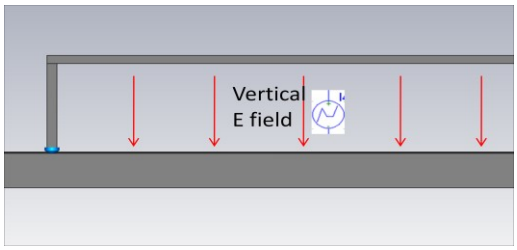

Fig 7: E field generating the current source

3. *Combine SPICE models of IC package and internal IC circuitry*

The IC package model, including both package parasitics and field coupling, and the model of the internal circuit components of the IC are combined in the final step. Fig 8 shows an example where a single pin model is connected to a model of the on-die power delivery network [4]. Once combined, the entire model can be simulated in SPICE, where the simulation can be done quickly and can include the full complexity of the IC circuitry.

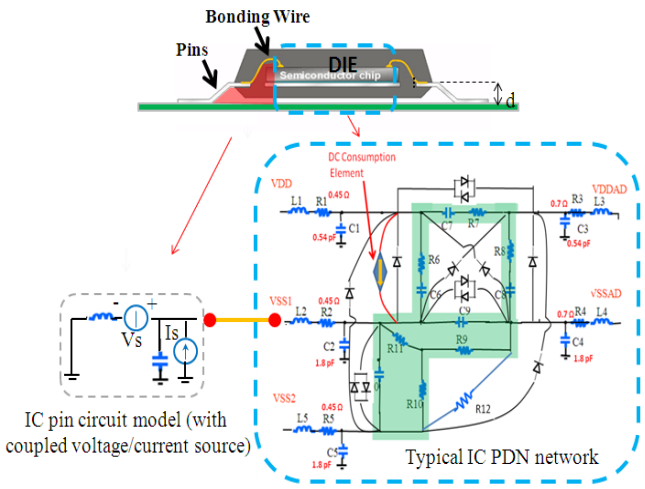

Fig 8: Complete circuit model of field coupling

III. Verification of the Proposed Method

Experiments were performed to verify the feasibility of the proposed modelling method. Validation was performed by first testing the accuracy of the full-wave model of the gun, then by testing the accuracy of the passive model of the IC package, then testing the overall estimate of energy coupled to

the IC. In these experiments, a "large" IC-like structure was built to mimic the geometry and circuitry of a real integrated circuit, shown in Fig 9. This structure was built to allow easier modification and measurement of the structure and to allow more precise knowledge of all internal circuitry than could be achieved for a real IC. For example, in this case the IC "die" can be created using known lumped-element components.

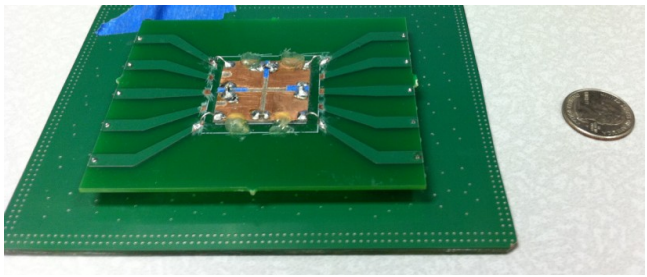

Fig 9: Photo of the large IC mimic.

1) Validation of the ESD gun model

As discussed above, the first step in the modelling method is to record the simulated electromagnetic field from the ESD generator. A Noise Ken ESS200 ESD gun was used in our experiments and simulations. A full wave model of the Noise Ken ESD gun was prepared in [2] and used again here. The reliability of the full wave ESD gun model was verified by comparing measurements and simulations of the noise voltage induced across a loop close to the ESD gun.

The test setup is shown in Fig 10. The loop had a radius of 13.5 mm and was placed 10 cm away from the tip of ESD gun. One end of the loop was terminated to the large ground plane, while the other end of the loop was connected to the inner conductor of an SMA connector mounted on the ground plane. The voltage across the SMA connector was measured using an oscilloscope.

Fig 11 compares the measured and simulated voltage across this loop. The simulated voltage closely matches the measurement.

2) Validation of passive package model.

In the second step, the passive model of the scaled IC (Fig 9) was validated. The scaled IC was built from two printed circuit boards (PCBs) as shown in Fig 12. The first PCB (on top) mimics the IC's die. A simple power distribution network (PDN) circuit was placed on this die for the following experiments. The second board mimics the package lead frame. This IC mimic was mounted on a third PCB (representing a PCB used in a real design). Although the scaled IC has ten "pins," only four of them were used in this experiment to represent VDD, VSS, VDDAD and VSSAD. The parasitic inductances and capacitances associated with this model were found through measurements here, though full-wave simulations of the package could have been used just as easily. This model was then combined with a model of the on-die power delivery network.

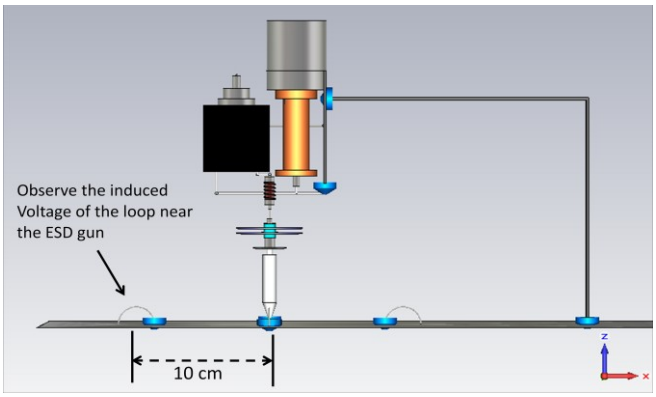

Fig 10: Full wave simulation model for detecting Induced loop voltage

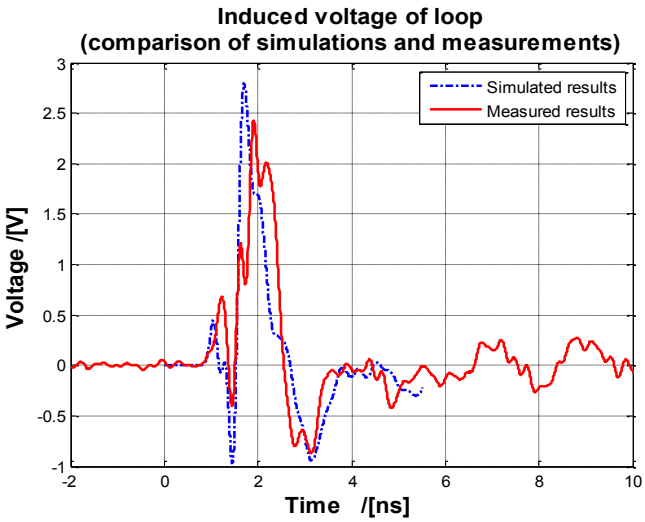

Fig 11: Comparison of measured and simulated induced voltage of a loop

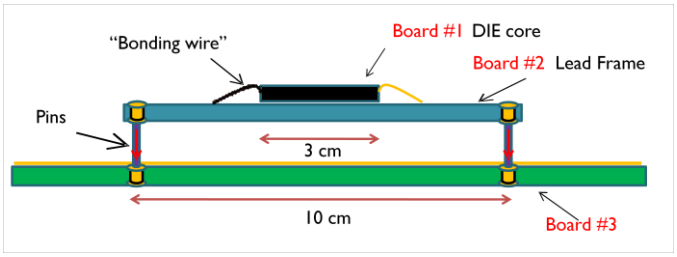

Fig 12: Side view of the IC mimic

The passive power delivery network used in these experiments is shown in Fig 13. It is similar to the circuit structure found in a real IC, as shown in [4]. The top copper layer of the "die" is divided into four patches, one each for VDD, VSS, VDDAD and VSSAD. Lumped components connect these separate patches to form a PDN circuit. The bottom layer of the die board is a solid floating piece of copper, mimicking the die pad in a typical IC package.

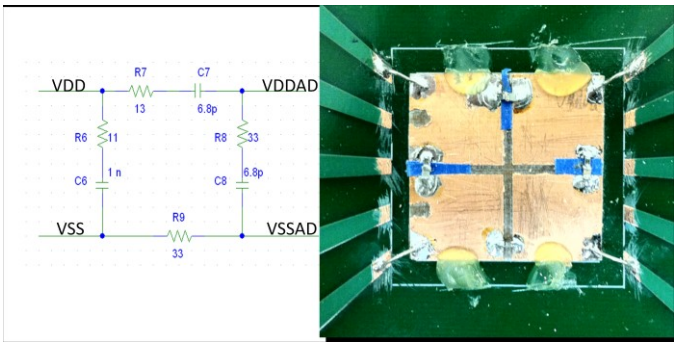

Fig 13: Power distribution network circuit implemented on the IC die mimic.

The overall SPICE model of the die is shown in Fig 14 and Fig 16. Fig 14 shows a simplified model to illustrate the models of the pins. Fig 16 shows the complete model, including the on-die power delivery network. These models also include the voltage and current sources, calculated from the incident electric and magnetic fields as shown in (2) and (4). In this case, because the IC mimic was so large and because the ESD gun generates energy at relatively high frequencies, a lumped element model of the pins was not sufficient. The final model shown in Fig 16 had to use transmission line models of the pins to accurately predict results.

The input impedance looking into the die model was validated experimentally. Input impedance was measured at the "VDD" pin as shown in Fig 14. Measured and simulated impedance is shown in Fig 15. The simulated values closely match those found through measurement.

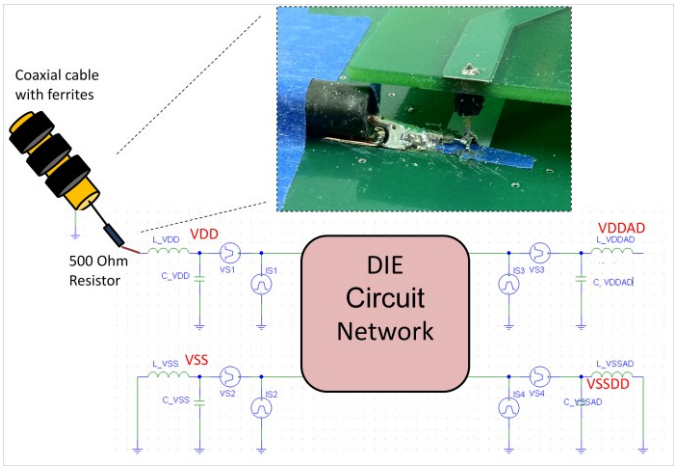

Fig 14: Measurement of the input impedance to the IC mimic.

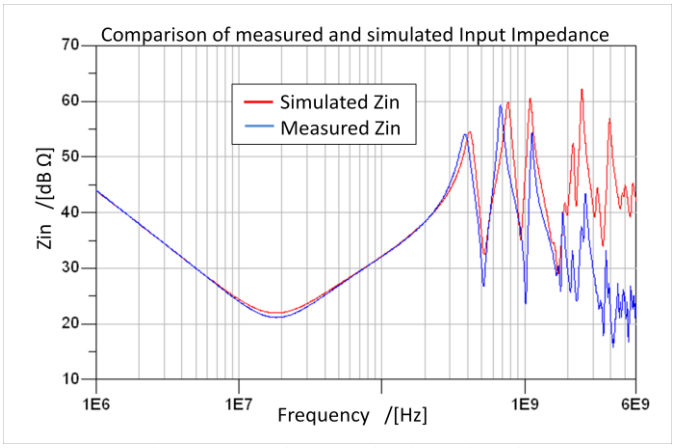

Fig 15: Measured and simulated input impedance

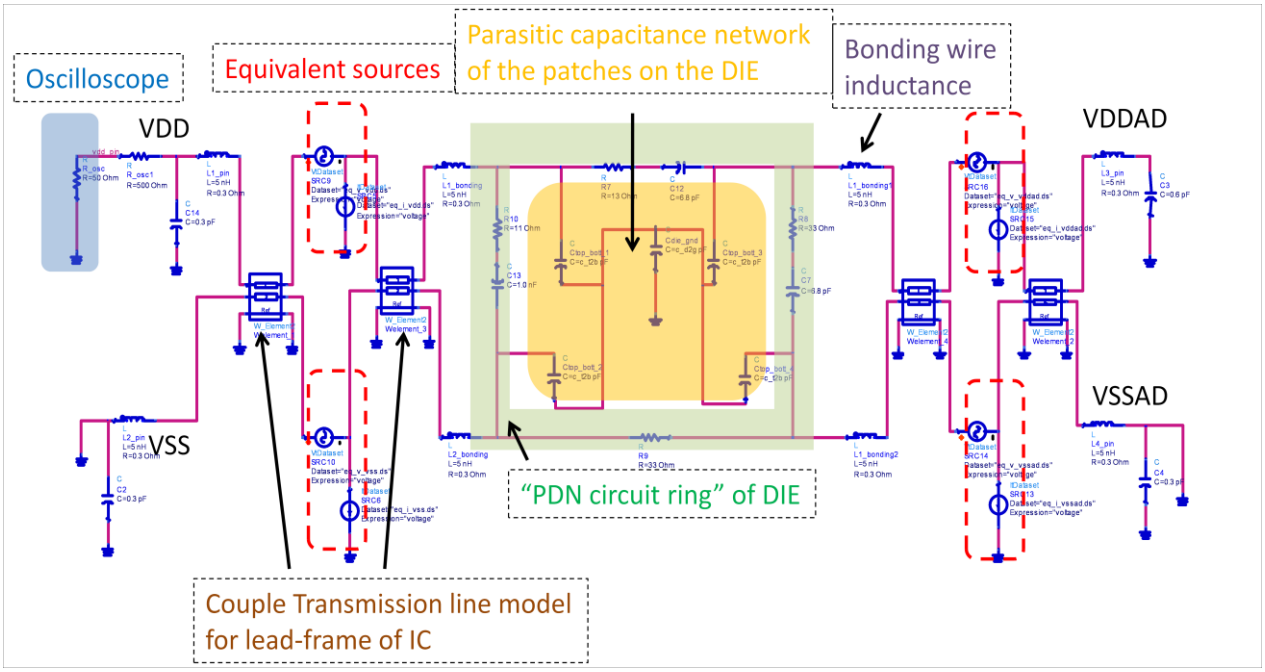

Fig 16: Complete SPICE circuit model for the IC, including coupled voltage and currents

3) Validation of overall coupling model.

The ability to predict coupling to the IC from the ESD gun was also validated experimentally. The measurement setup is shown in Fig 17. The distance between the tip of the ESD gun and the edge of the IC mimic was 10 cm. The voltage on the pins of the IC was measured via a coaxial cable connected in series to the pin through a 500 ohm resistor as shown in Fig 14. The simulated and measured results are shown in Fig 18. In general, the power level waveform trend match well, although do not match across the entire time scale, most likely because of a mismatch in the impedance between the actual and IC and the model. We believe these inaccuracies can be overcome with more careful modelling of the package impedances and more careful implementation of the coupled currents and voltages into the model, in a way that better accounts for the transmission-line characteristics of the model.

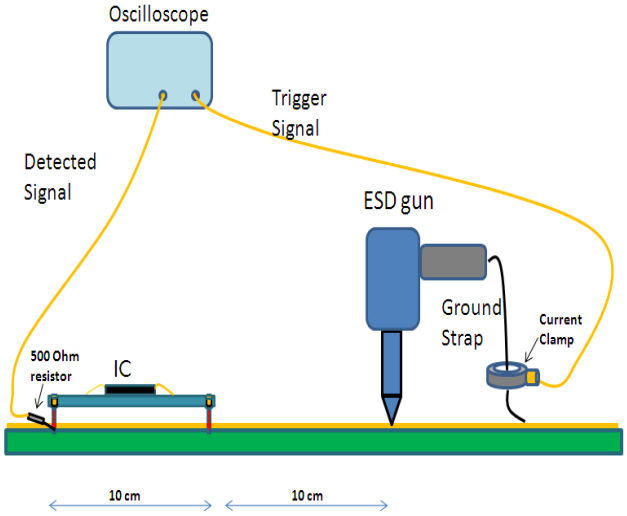

Fig 17: Measurement setup for ESD test on scaled IC

IV. Conclusion

A method was proposed to quickly estimate the electric and magnetic field coupling from an ESD gun to an IC. This method can potentially predict the coupling much faster than a full-wave simulation approach and can account for the full complexity of the on-die circuitry. A major advantage of this technique over pure full wave simulations is that it can allow the designer to better explore variations in the experimental setup and thus the variability in the coupled voltages and currents. Changing the position of the IC relative to the ESD gun is as simple as changing the electric or magnetic fields used to calculate the equivalent voltage and current sources in the package model. No additional full-wave simulations are required. Different ESD gun configurations (e.g. length or connection of the ESD strap) can be simulated in a full-wave model once and used over-and-over. Similarly, changes to the IC, to test improvements to the ESD circuitry, do not require any additional full-wave simulations and can be conducted entirely in SPICE. Preliminary results show reasonable correlation between simulated and measured voltages found in a IC-like package during an ESD event.

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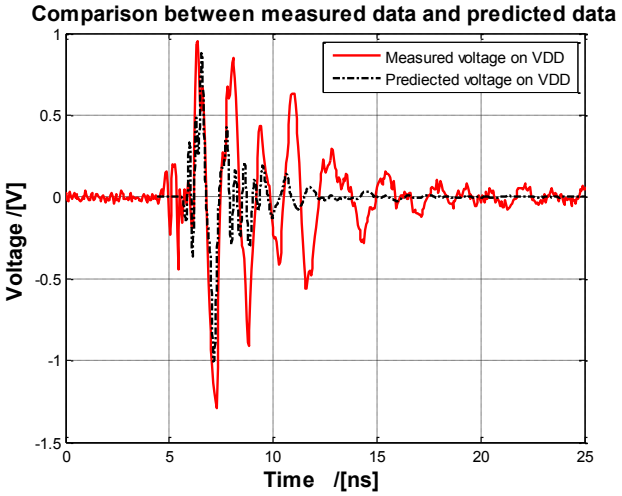

Fig 18: Measured and predicted voltage on VDD pin

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