DesignCon 2006

Finding the root cause of an ESD upset event

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Abstract

System level Electrostatic Discharges (ESD) can lead to soft-errors (e.g., bit-errors, wrong resets etc.). By this talk we try to offer guidance in finding the root cause of upsets frequently observed in immunity testing (e.g., ESD, EFT). At first a description of the ESD discharge process is given. It provides the necessary background for correctly analyzing ESD failures. Local scanning and in-circuit measurement techniques are explained. Further, it is shown how PCB scanning results, revealing local sensitivities, can be used for the characterization and optimization of circuit and ICs design and software for minimizing unwanted responses to soft-error causing noise. A series of measurements of such noise voltages coupled into a sensitive trace are presented.

Biography

David Pommerenke is a faculty member at the University Missouri Rolla, EMC laboratory. His interest are EMC, especially circuit related aspects, SI and the design of measurement methods and instrumentation. He is US representative in the IEC group that sets the IEC 61000-4-2 ESD test standard.

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Opening questions: "It has failed, why?"

Often engineers get involved into system level ESD through questions like "how to fix an ESD problem on a EUT?" by asking themselves "which design choices will prevent ESD problems?", or by thinking about how do I optimize an IC design for best system level ESD performance?" and "how do system level and IC level correlate?" To help answer such questions first fundamentals of ESD are reviled. Secondly, an immunity scanning method (fig.1) is introduced. In most cases it revealed the root cause of system level ESD problems and allows characterizing of IC immunity performance. In addition to illustrating the state of the art, an assessment is given on the limits of the understanding of ESD upsets in electronic systems. A variety of examples illustrates the approach.

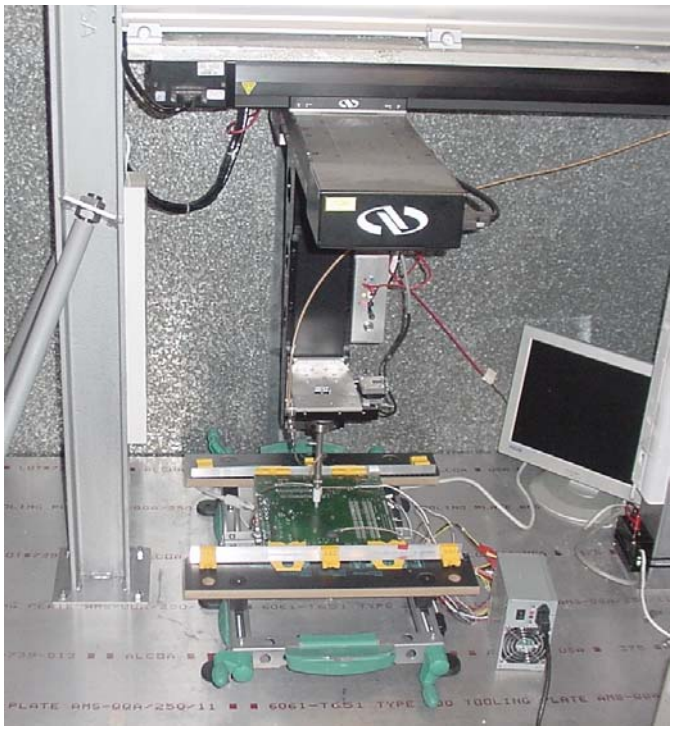

Fig. 1: *Immunity Scanning System [1, 2].*

Needed background: Events during an ESD discharge

At first, let's clarify the broader context of this paper and how it relates to other, mainly IC related information on ESD engineers are often are confronted with.

ESD occurs when two objects having different potentials approach close enough such that sparking occurs. This is a complex event. Understanding is simplified if it is broken down into four main phases:

- Electrostatics, describing the charging and charge distribution prior to the breakdown.
- Physics of sparking, describing the development of the conductivity in the arc.
- Fast transient electromangnetics; during the first phase of the discharge EM-waves travel on the EUT and on the human. Local differences and temporal changes are strong. Consequently, the structure is electrically large: antenna theory, shielding and coupling are the appropriate methods for describing ESD in this phase. Picture this phase as if a 3 GHz pulse impinges on the EUT.
- Slower currents and charge redistribution; after the first phase current derivatives and voltage derivatives have been reduced by radiation and reflection to levels that the dominating frequencies are low enough, such that the structure can be treated as being electrically small. A description by equivalent circuits is suitable in this phase of the discharge.

The fast transient electromagnetic phase is the most challenging, but it is the root cause for most of the soft-errors observed. Consequently, this article will concentrate on voltages and currents present during this phase of the discharge.

Use care: IC level vs. System Level Standards

For quantifying ESD robustness, a wide variety of discharge scenarios have been used as base for standards. It is important to distinguish between system level and IC ESD level standards. Please also note that a variety of IC immunity standards are being developed. Please see [3,4,5] for IC level immunity standards that are being developed.

Reference Event	Standard/ Model	Failure indication	Main parameters
Human discharging through a small piece of metal	IEC 61000-4-2	Soft-error (upset, reset) and Hard-error (damage)	2-15 kV 0.7-1ns rise time 3.75 A/kV peak current
Discharge of a metallic furniture, e.g., a lab card	Furniture discharge (ANSI C63.16)	Soft-error (upset, reset) and Hard-error (damage)	Weakly damped oscillation, typically 50-200 MHz, very large initial current derivative, but 10-90% rise time a few nanoseconds, currents up to 10 A per kV charge voltage

Table 1: *Important system level ESD standards*

Manufacturers of ICs usually provide ESD test information. However, this information is based on IC level standards (HBM, CDM, MM and latch up). The application of IC level standards to system level testing is often confusing and should be clarified.

Only in some circumstances IC level standards allow to predict system level performance. The main reason is that most IC level standards do not test for soft-errors (bit errors, upsets, unwanted resets etc.). They only test if the ICs are damaged by ESD. In contrast, system level test standards are applied to operating systems while observing the functionality of the system in addition to observing for damage. Consequently, one cannot use IC level ESD information for analyzing system level soft-error problems. Latch-up must be considered a special case. An IC may go into latch-up, but survive. During the latch-up the logical function is interrupted, such that the observer will observe only a soft-error, but no damage.

If a system level test leads to hard errors then it is possible to use the IC level test information for analyzing system level results. However, sufficient caution needs to be applied. A careful look at the underlying models and test levels is needed. For example: The system level human discharge model is based on a discharge of a human via a piece of metal, while the IC level model is based on a discharge from the skin to the grounded IC. This leads to vastly different model parameters. To illustrate an example, the IC level and the system level HBM standards are contrasted below:

IC level HBM (human body model)	System level HBM
C = 150 pF	C=150 pF
R_series = 1500	R_series = 330
Trise < 5 ns	Trise 850 ps
Voltage usually less than 4000 V	Most tests up to 8000V
Only damage to the IC	System upset and damage

Table 2: *Comparison of IC and system level ESD standards based on ESD by humans.*

Events during an ESD: From Statics to GHz propagation

The aforementioned different phases of an ESD need to be reviewed in greater detail to counteract the often met misunderstanding that ESD can be described in terms of static's. ESD is not only a very broadband event, but an ESD tests is the combination of different physical stresses applied to a system. Depending on the EUT and test point, totally different mechanisms may lead to damage or an upset.

Human ESD: The beginning scenario is a human holding a small piece of metal (e.g., a key, ring, screwdriver). He has been charged and is approaching a grounded part of a system.

The discharge of a human (via a small, hand-held metal piece) is bases for the current waveform of the most often used IEC 61000-4-2 [6] standard. The ESD process is associated with strong electromagnetic fields (for 5kV discharge: 18A peak current, rise times 850ps, about 10kV/m and 25 A/m in 10cm distance [7, 8]) and large currents.

1. Prior to the discharge an electrostatic field exists. As there is no (or only very little current) flowing, no relevant magnetic field is present
2. Once the distance is sufficiently small, a dielectric breakdown will occur; the electrostatic field starts collapsing. It collapses down to about 25-40V within 50ps – 5 ns. The collapse time is depending on arc parameters, voltage etc. [2].
3. A current starts flowing on the metal part and the EUT. The foremost current front expands with the velocity of light. For example, within about 0.8 ns it has reached the arm of the person. The current will be expanding further on the EUT and the arm. It will experience reflections and losses due to radiation and resistance, leading to a complex pattern of current density of the EUT and the person. During this phase the person and the EUT act as antennas. This phase is about 10 ns long. The highest frequency components of the current will be attenuated mainly due to radiation leading to a smoother current (=less high frequency).
4. As the higher frequency components do not dominate the anymore a description as equivalent circuit is possible for a time frame from about 10ns until the body reaches a new electrostatic equilibrium. The remaining charge may not be zero, as the arc might extinguish before this has been reached. If the hand is approaching the EUT further, a second discharge will occur (at a lower voltage now). This can lead to a sequence of ESDs, each one at a lower voltage, but each one having a faster rise time (partially attributed to the lower voltage).

During each discharge, an observer located on some point of the hand, body or EUT will observe a charge density prior to the discharge, during the discharge phase a fast changing current and after the discharge a small remaining charge.

From antenna theory it is known that time varying charge densities and currents will cause radiated fields. In close proximity the fields are dominated by the current and the charge directly, and in larger distance the current and charge time derivative will determine the fields. The transition region is more complex. Measurements and simulations have shown that transient fields of ESD, at least for the most disturbing first nanoseconds already reach far field conditions at a distance of 10-20 cm from the point of arcing [7,8,9]. The transient fields of a human-metal ESD are part of the ESD process and should not be considered as “unwanted radiation”, however, excessive transient fields of ESD generators might be considered as such.

ESD Generator

During ESD testing ESD generators are used instead of human discharges. An ideal ESD generator would reproduce the currents and fields of a human ESD. The processes that occur within an ESD generator have some important differences. For reasons of reproducibility of the discharge current the arcing between the EUT and the generator has been substituted by a well controlled discharge within a relay. However, within the relay the voltage collapse occurs in about 50 ps, causing strong high frequency fields.

To achieve a current rise-time of about 700-1000ps at the point at which the ESD generator meets the EUT low pass filtering is performed. However, the radiation of an ESD generator is governed by all currents, including the fast changing currents within the relay. They increase the high frequency content of ESD generator transient fields beyond the transient fields of an equivalent (=same current rise time and peak value at the point of discharge) human-metal ESD. By how much? This depends on the design of the generator. As consequence one has observed

variation in test results for upset related failures of up to 1:4 ([10]) if different brand ESD generators have been used [1,11,13]. These differences occur mainly if the EUT is sensitive to high frequency fields > 1 GHz. The IEC TC77b is aware of these problems and working on an improved standard.

EUT reaction to ESD testing

During an ESD test the reaction of an EUT to a broad range of electrical disturbances is tested. The range includes: Voltage for dielectric breakdown, secondary breakdown at a gaps away from the injection point, current for RI drop, Magnetic field for L di/dt drop, Magnetic and electric fields for induced voltage, fields can be in far and in near field. In this regard an ESD test differs from EMI testing. ESD testing combines multiple tests into one.

Some examples of EUT failures due to different disturbances of the ESD test are:

- Discharge into a connector PIN causing damage to an IC.
  In the above example the **energy dissipated** in the IC, the **maximum current** or the charged transferred through the IC, or the **voltage** that caused a gate-oxid failure will most likely determine the damage threshold.
- Discharge through a gap in a plastic enclosure allowing a spark to reach an IC.
  In this case the ESD test did test the **dielectric breakdown** strength of the gap through the plastic seam.
- Discharge to a chassis causing the system contained in the chassis to upset.
  In this example, most likely the **transient fields** of the ESD event did couple into traces, wires or directly into ICs of the system causing voltages or currents that upset the logical function of the system.

In summary, vastly different processes can lead to an ESD failure on a product. Testing, reporting and reading of reports needs to be performed with great care.

Coupling and induced voltages

The coupling mechanism from the current within the ESD generator to the fields is dominated by the current's time derivative even at relatively moderate distances of e.g., 20 cm. Further, the coupling between the field and a wire, trace or IC is a function of the rate of change of the electric and the magnetic field. In summary: Both the field creation and the induction process contain time derivative. This leads to different pulse shapes for the current at the discharge tip compared with the wave shape of the induced voltages in traces. Usually, the induced voltages in traces are pulses having a width much more narrow than the initial ESD discharge current as defined in the standard. They may exhibit ringing. While there is a wealth of information on shielding and on coupling to traces, both for ESD and other immunity testing. But no one has yet assembled this information to provide a good guideline that allows estimating the voltages induced in given trace or cable geometries for typical enclosures during ESD testing. An ongoing investigation in our group tries to close this gap.

Finding the root cause of an ESD problem

Shielding is an option for solving ESD problems; however it is often not the most economical, especially if the production volume is large. In these cases it more economical to locate the affected nets; beginning from the following questions:

1. How repeatable is the test results? If a result is not repeatable, it will be very difficult to prove or disprove the success of countermeasures.
2. Is it a soft- or a hard-error? In all cases, except of secondary breakdown it is quite easy to locate the path for an ESD if a part is damaged. However, soft-errors leave few if any traces.
3. At which discharge point did the error occur? The discharge point might be close to the affected part of the circuit, or it might be close to an opening (or cable) that guides the wave to the affected part of the circuit.
4. Was the testing done in contact or in air discharge mode? Contact mode testing is by far more repeatable and should be used whenever possible.

Which net is affected?

Now let us assume it is a soft-error. The next step would be to localize the affected net.

One might approach this by measuring voltages inside the EUT at some critical traces while applying ESD. This is very difficult and is bound to fail in most cases due to the large currents flowing on the probing system. However, if fully shielded semi-rigid cables are used, plenty of ferrites are placed on them and if the oscilloscope is in a shielded enclosure then such measurement have been conducted with success.

The concept of field mapping is well established for studying electromagnetic emissions from PCB. Susceptibility scanning is the inverse process: It locates local sensitivities. An ESD susceptibility scanner (fig.1) has been developed [1,2]. It allows the quantification of noise sensitivity of PCBs and ICs. It performs automatic identification the ESD sensitive Pins and Nets in non-destructive ESD failure testing. This allows testing the effect of different I/O structures, IC technologies and on-board filter structures.

The ESD scanning system has the following components:

Three dimensional positioner; High voltage pulse generators; ESD pulse injection probes; and EUT feedback and control software.

The values shown (e.g. indicated by color or height) on a susceptibility map show the lowest ESD failure level that lead to a system malfunction. They are scaled in pulse generator setting, not in induced voltages as these are a function of the local geometry and the driver and receiver loadings. Peaks (or red color) in the map indicate the points which are most susceptible to the ESD event.

A fast rising pulse is applied to the scanning probe and the probe is moved to the surface of the EUT. The operational status of the EUT is monitored by the software and any upset of the EUT is recorded to generate the ESD susceptibility map of that EUT. Of course, the software monitoring is a function of the EUT tested. Relative to hand scanning a better reproducibility of the results is achieved that allows the systematic comparison of PCB or IC modifications.

The procedure to characterize the ESD susceptibility of a EUT is as follows:

1. **Course scan:** Using different probes, scans are performed at larger scan resolution and higher scan speeds. An initial ESD susceptibility map is generated.
2. **Fine scan:** Sensitive areas are analyzed using smaller probes and finer scan resolution.
3. **Trace voltage measurement:** The sensitive traces are analyzed and voltage measuring probes are attached to the trace to capture the voltages while injecting into the traces.
4. **Countermeasures:** After understanding the electrical function of the net countermeasures can be designed.

Typical results, before and after modifying a PCB are shown in the following figures.

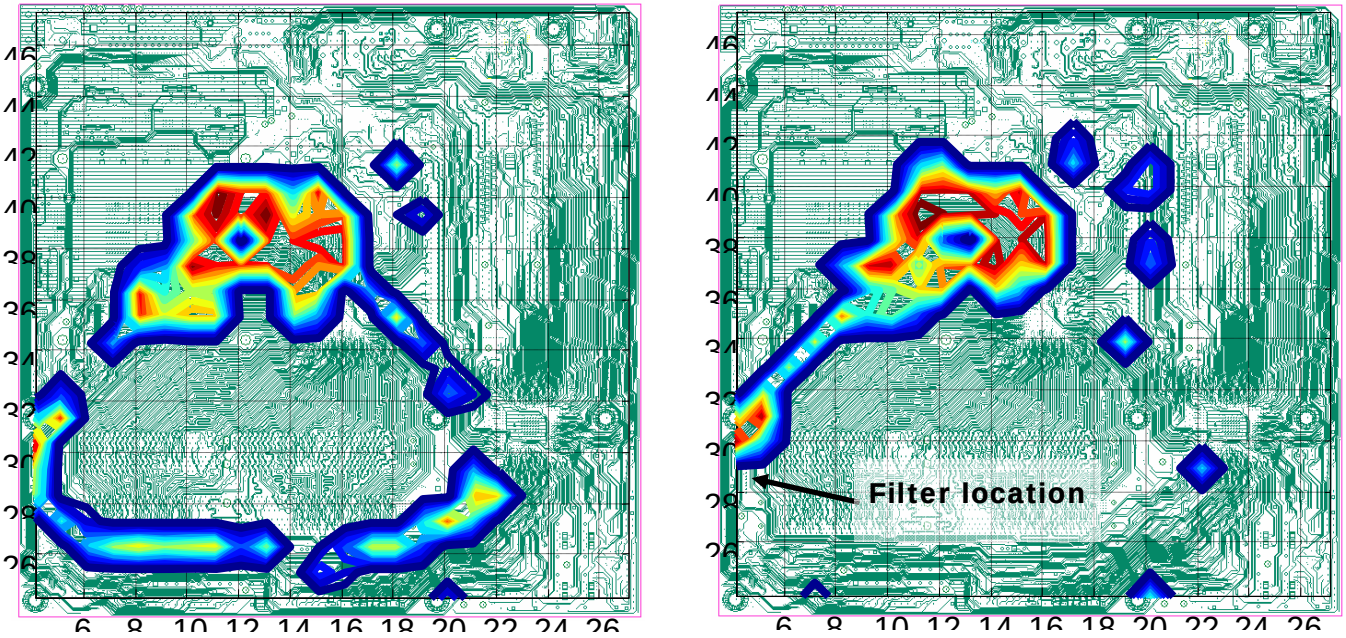

Figure 2: *ESD susceptibility map of an EUT. Left: Before filtering the trace, Right re-scan after inserting an RC filter into the trace.*

Figure 2 is the two dimensional view of the ESD susceptibility map of the EUT obtained by using a loop probe before and after filtering a trace. To identify the traces and nets sensitive to ESD, better resolution scanning is often required. For example, a small H field probe or direct injection probing will narrow down the affected area and provide inside into the nature of the circuit response. Typical probes range is size from 10 mm to less than 1 mm.

Fig. 3 illustrate this: Three sensitive nets have been identified in area No.1. It is interesting to note that 3 nets are more than 10x as sensitive than any other net on the board. This is not an untypical result and it reinforces the approach of locally improving a board or an IC over shielding the system. An RC filter has been introduced into net 2. The signal on net-2 is a slow signal (status line) such that low-pass filtering does not inhibit the functionality of the system.

This example is typical for PCB layouts: While clock and data bus traces are routed very carefully for EMI and SI reasons there is less or no care given to status lines. They may even connect boards via low quality connectors or are routed close to the board edges. In this way,

good antennas are formed. From an EMI perspective it is only important that the status line carries a slow signal, however from an immunity point of view it is important how fast a trace can react to induced noise, no matter how slow (of low frequency) the intended signal is.

Introducing the RC-filter reduces the sensitivity of the net (fig. 2).

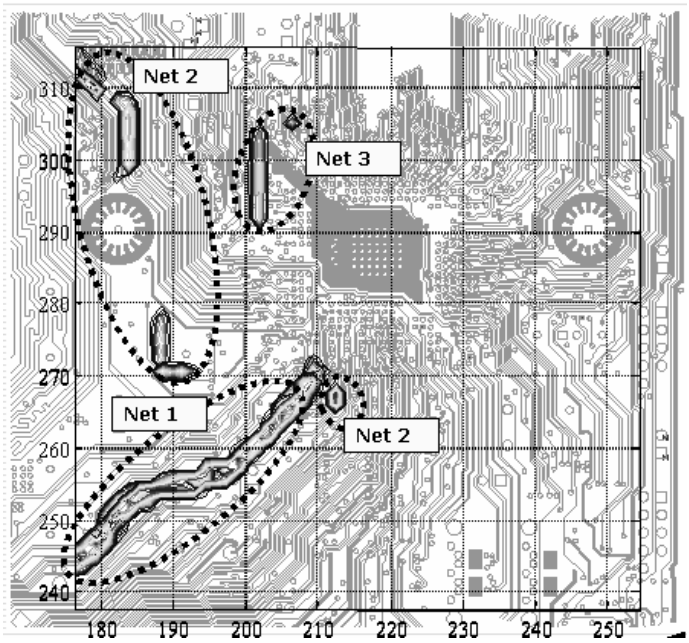

Figure 3: *Three ESD sensitive nets of the EUT.*

Pulse generation

To achieve scanning results that reflect system level performance noise needs to be injected that equals in its main characteristics the voltages and currents induced by system level testing. As mentioned in the introductory part: The process of penetrating shielding and coupling is a high pass filtering, causing the induced voltages to be pulses more narrow than the original currents pulse of the ESD.

Two types of pulses are used for the noise injection:

Transmission line pulser

A TLP (transmission line pulse generator) creates a square wave pulse. It charges a 50 ohm cable while the relay is off and produces a high voltage impulse with about 900 ps rise-time (10-90%, 500ps 20-80%). The maximal charge voltage is presently 5000V. The pulse length can be changed by adjusting the transmission line length. Usually a few nanoseconds are sufficient for ESD testing purpose as the rising part dominates the high frequency components. TLP ESD testing has the following advantages over ESD simulator testing:

- The voltage and current are well defined
- The fields produced at the probes are well defined, i.e., they are not as complex as the fields and radiation produced by ESD simulators.
- Near field probing of the boards is possible

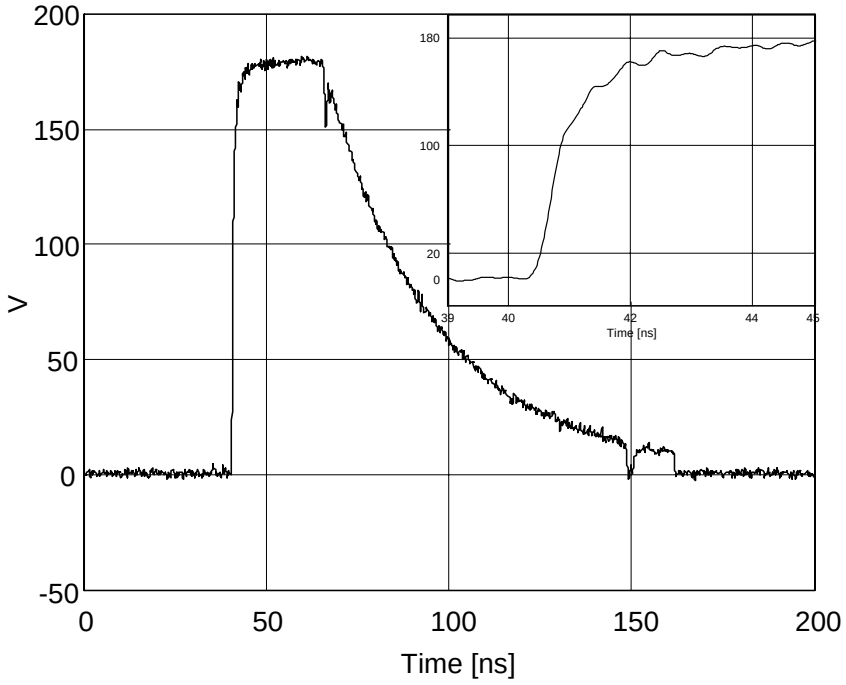

Figure 4: *The output of the high voltage transmission line pulse generator. The rise time of the rectangular pulse is 900 ps. The data shown was taken at 400V charge voltage. The maximum charge voltage is 5000 V. The measurement has been performed using a TDS7404 oscilloscope (4GHz bandwidth, 20G Sa/s). The fall time has been increased to distinguish polarity effects if the coupling from the TLP to the system follows a derivative function (e.g., inductive coupling).*

Narrow Pulse Probe

A different pulse generator is used to inject narrow pulses of shorter rise time. This is mainly done to obtain a often non-linear “impulse response” of an IC input. A transmission line or a PCB patch is charged and discharged via a mercury wetted relay. The relay has been modified to improve the pulse shape and pulse repeatability. The mercury relay is small, which allows the pulse generation to be done close to the probes to reduce the effect of cable losses on the rise time.

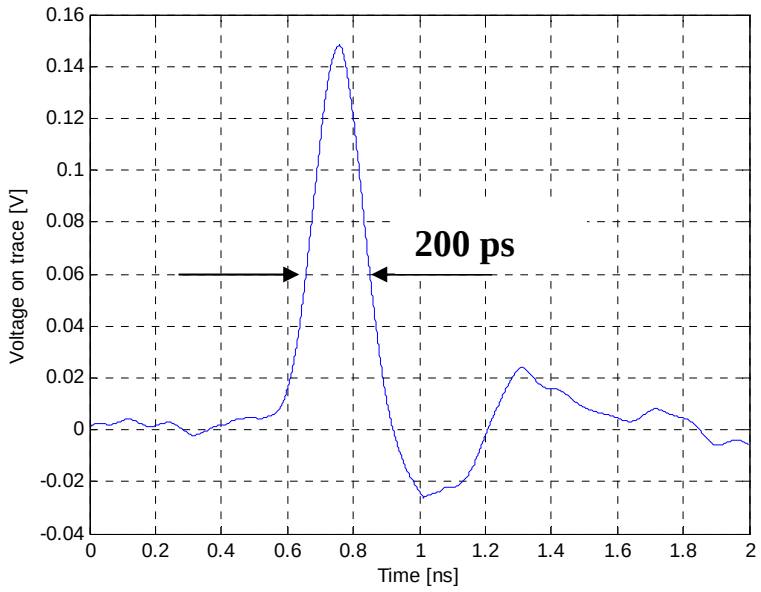

Figure 5: *The output of the narrow pulse generator measured into a 50 Ohm trace terminated at both ends. The generator can provide up to 30V pulses. Other pulse generators provide pulse widths of less than 130 ps (at half amplitude).*

Injection probes

Different ESD pulse injection probes are connected to the output of the TLP to simulate a variety of ESD event coupling mechanisms. The following injection probes are used in the ESD susceptibility scanning system.

- Flat and Vertical H field coupling probe
- E field coupling probe
- Direct injection probe

Fig. 6 depicts the fundamental concepts of these probes.

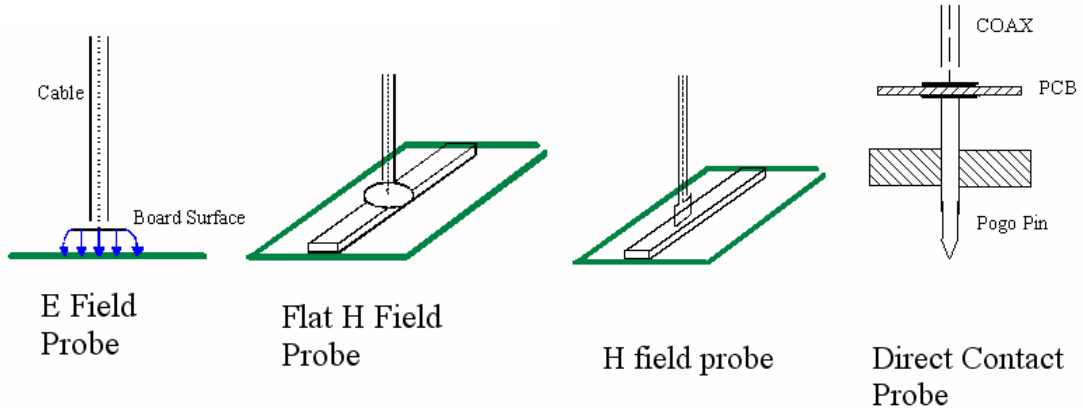

Fig. 6: *Different probes used for noise injection.*

E field probe consists of a metal plate connected to the inner connector of a SMA cable. It simulates the capacitive coupling. The return current path is provided by the displacement current between the outer shield of the coax and the PCB.

Flat H field probe is a small loop attached to a semi-rigid cable. The loop is parallel to the scanned PCB surface.

H field probe is a small loop attached to a semi-rigid cable. The loop is perpendicular to the trace and the PCB board surface. It simulates the transient ESD magnetic field.

Direct injection probe is a probe composed of a coaxial cable and a shunt capacitance made from the upper layer and lower layer of a PCB board. A pogo pin, which is used to inject current directly into traces and pins on the EUT, is connected to the lower layer of the PCB.

A test board, using a narrow 50 Ohm trace is used to characterize the injection probes by measuring the coupled noise voltages, fig. 7.

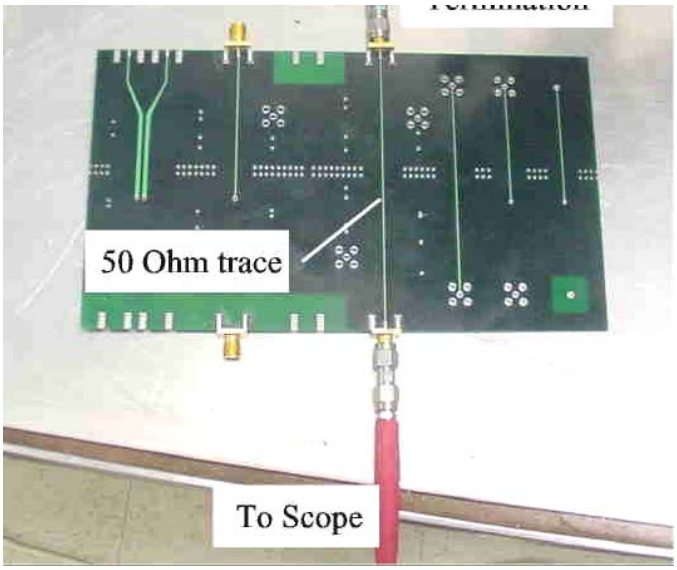

Fig. 7: *The test board used to measure the voltage induced and current injected. The PCB trace dimensions are as follows: Length = 4 inches, Height over the ground plane = 10 mil, Trace width = 18 mil, Copper thickness = ½ oz = 0.675 mil.*

The pulse from the TLP is applied to the H field probe and the noise voltage measured at both ends of the trace. Comparing both voltages allows distinguishing between E and H-field coupling.

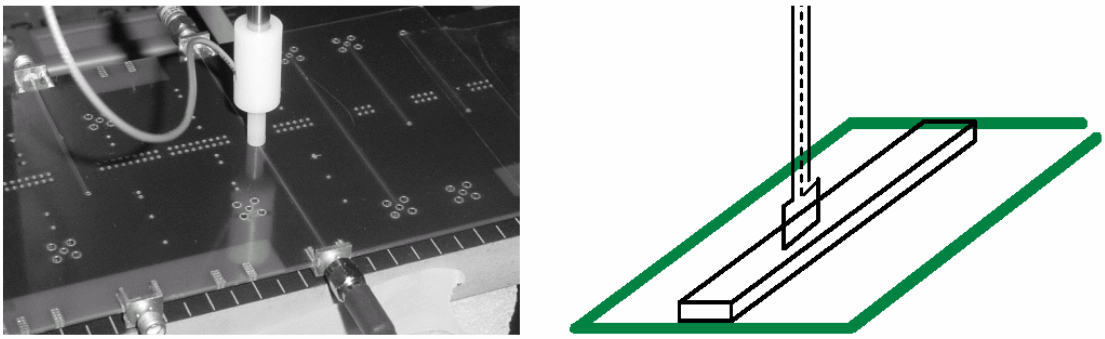

Fig. 8: Test setup and sketch of the coupling orientation for characterization of one H-field probe coupling.

Figure 8 shows the characterization the of H field probe. The coupling between the H field probe and the trace has two components: Electrical field coupling (Capacitive coupling) and Magnetic field coupling (Inductive coupling). The later should be dominating. The data in figure 9 shows the mixed coupling mechanism of the H field probe.

The results for the direct injection probe are shown fig. 10. The probe was connected via a pogo pin to the trace while the rectangular pulse from the TLP is applied.

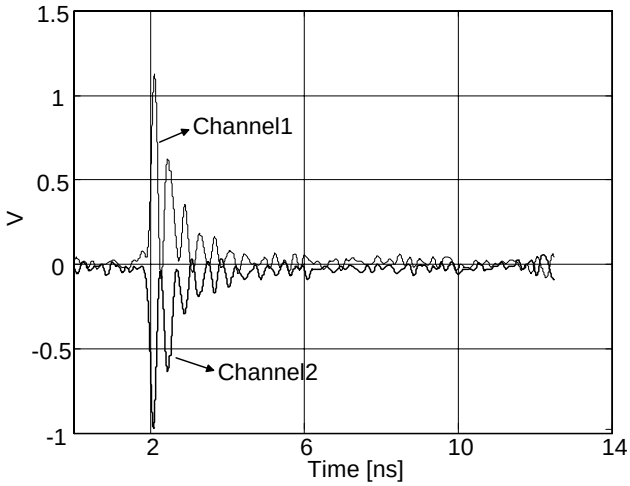

Fig. 9: Measured noise voltage coupled by the H field probe. The charge voltage to the TLP is set to 400V. Clearly, the magnetic coupling dominates (inverse voltages at both ends of the trace).

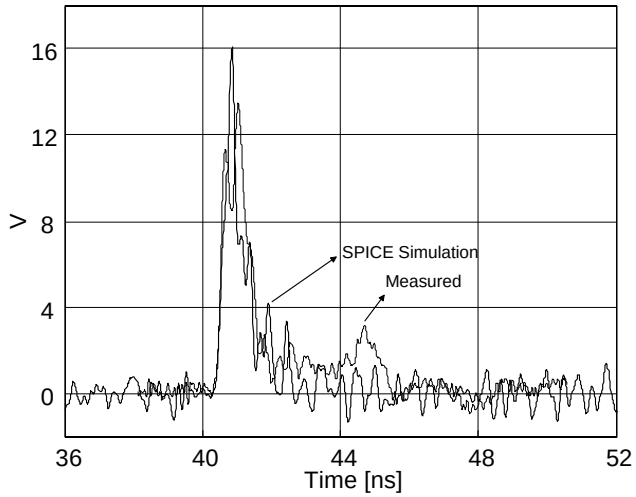

Fig. 10: *Measured noise voltage coupled by the direct contact probe. The charge voltage at the TLP was set to 400V. The dotted line is a simulation result of the capacitive direct contact coupling. Note: The noise in the simulation is caused by using a measured waveform as excitation.*

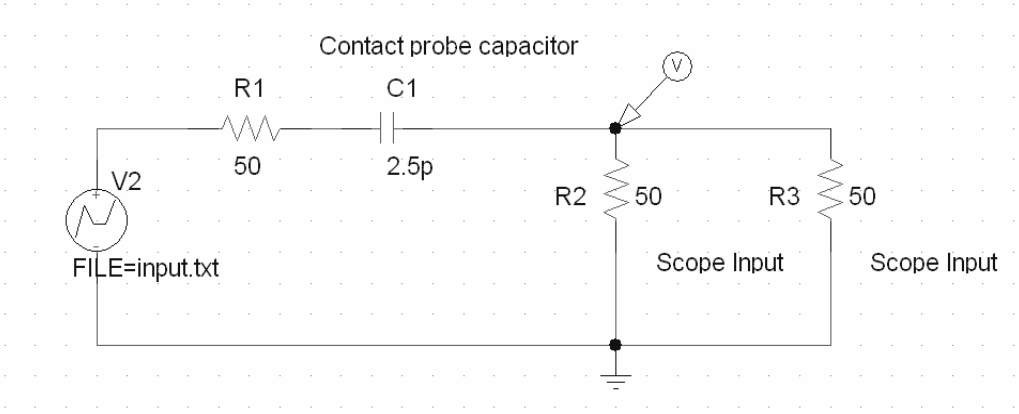

Fig. 11: *The simplified SPICE model of the direct contact probe.*

The data in figure 11 clearly shows the capacitive coupling mechanism of the direct contact probe.

In summary, a variety of probes is useful to reflect different localization ability, first for a coarse scan, till identifying single traces in very dense PCB and to reveal disturbances that are based on either electric or on magnetic field coupling.

Direct coupling into the IC

More and more functionality is packed into ICs. Some PCBs contain mainly ICs connected by buried traces and a few power distribution and indicator components. In such cases it is very difficult to introduce PCB countermeasures. Short and buried traces do not form good antennas. The sensitivity is often dominated by direct coupling into the ICs. An example of such a situation is shown in fig. 12. The most sensitive location on the board was above a prototype IC. Careful

IC and package design and methods for the quantification of the soft error sensitivity will allow improving the robustness of ICs.

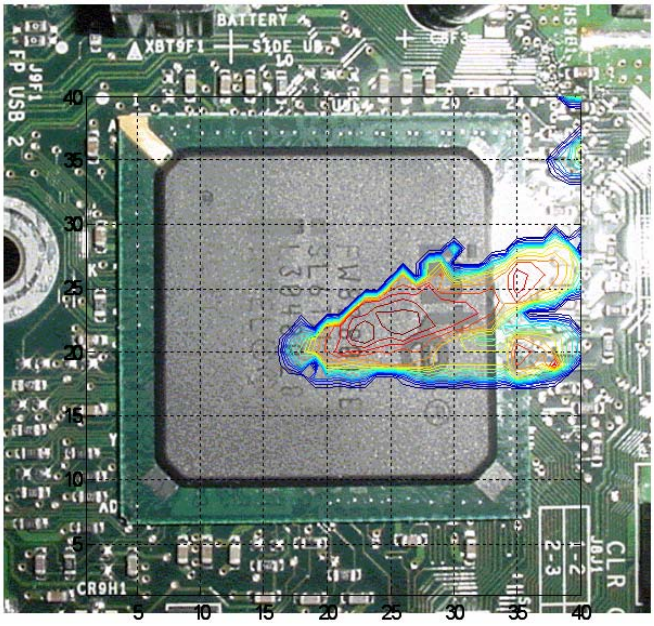

Fig. 12: *ESD susceptibility map of a fast CMOS IC, scan area: 40 mm x 40 mm.*

The data shown in figures 12 show scanning results using 0.2 mm resolution. Direct coupling into the IC dominates the sensitivity. The exact mechanism of the coupling is not known, but the use of bond wires and the location of the most sensitive area suggests coupling into bond wires.

Comparison of IC designs

Often one has the choice between two ICs having identical functionality, but having different immunity performance. This may be a result of different vendors, different stepping or process technology. Below is an example of such a comparison: Two functional identical prototype ICs have been compared. In the first step scanning identified the sensitive traces, in the second step direct injection of pulses into these traces compared the IC designs. The numbers in the left table are voltages settings on the transmission line pulser using a 1x1mm loop as injection method. Two traces have significantly different crash levels (pin I and D).

Pin Name	Mod B (new)	Mod A (old)
I	1000	➢4000
P	600	800
S	>4000	>4000
A	>4000	> 4000
B	>4000	>4000
D	1000	➢4000

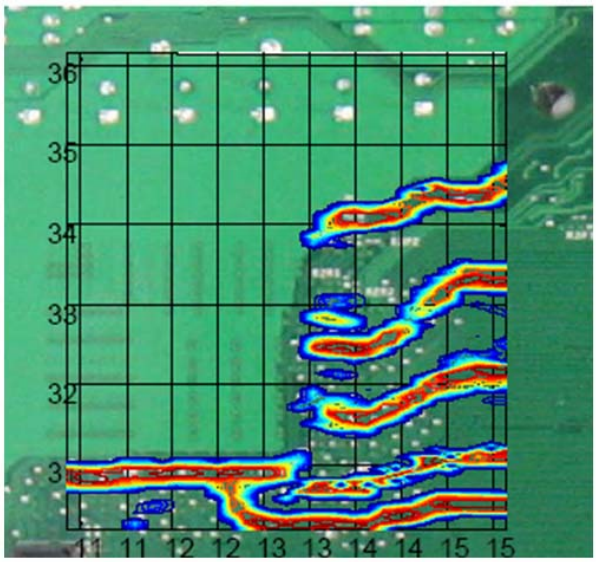

Fig. 13: *Comparison of two ICs for ESD susceptibility. The left table shows the upset levels expressed in voltage setting on the TLP when using a small loop as injection device. The right plot shows the sensitive trace locations after identification using scanning.*

Noise voltages on nets

An advantage of the locally injecting is the ability to measure voltages on traces. Compared to full ESD testing the common mode excitation is strongly reduced. Most active probes will not be suitable for measuring the noise voltages, not as a result of bandwidth limitation, but as consequence of unwanted coupling into the unshielded area and by coupling through the probe shielding and the connecting cables. Both contributions may induce an unacceptably large voltage into the measurement system, masking the waveform of interest.

A probing method that reduces the loop area size, but loads the circuit stronger is mounting a coax cable via a 470 Ohm SMT resistor onto the trace. Is has been applied in many situations for capturing noise voltages, see fig. 14. Resistors values larger than about 1000 Ohm will cause difficulties in achieving a flat frequency response of the probing due to the ratio of parasitic capacitances and resistances. Lower resistance values, e.g., 150 Ohm might load the circuit too strongly.

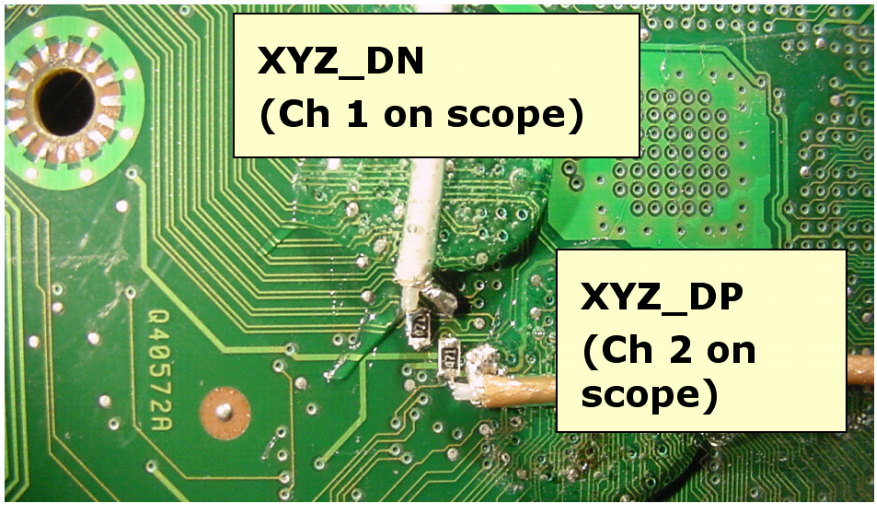

Figure 14: *The setup to measure the noise voltages on two traces. Two 470 Ohm resistors connect the traces via coax cable to an oscilloscope.*

How noise leads to bit errors

The most obvious reason for a bit error is given if the induced voltages is below VCC but above VSS and passes a threshold level to stay above it long enough to be detected by the IC as a legal transition. Other possibilities exist:

1. An input has a response speed much faster than needed for functionality reasons. This occurs often, if, e.g., the same I/O buffers are used for fast inputs as well as for slow status lines.
2. A differential system is pushed against its maximal common mode signal range, leading to a bit error.
3. An ESD protection circuit may trigger on a very narrow pulse. The circuit has a finite recovery time. The original ESD pulse may not be long enough to be detected as a legal transition, but the recovery of the ESD protection circuit will lengthen the effect of the ESD, causing a bit error.
4. An IC may go into latch-up and recover from latch-up. The user may not notice the momentary latch-up condition; instead recognize only an upset in the logical processing.

Of the aforementioned cases, case #1 and #2 have been observed by us frequently. However, we do not know how often case #3 and case #4 occur. Our ongoing research is trying to answer this question.

Example case #1: Status line reacting very quickly

In a prototype system it was observed that system level ESD results strongly dependent on the stepping of one IC. The response of a specific status line was measured, see fig. 15.

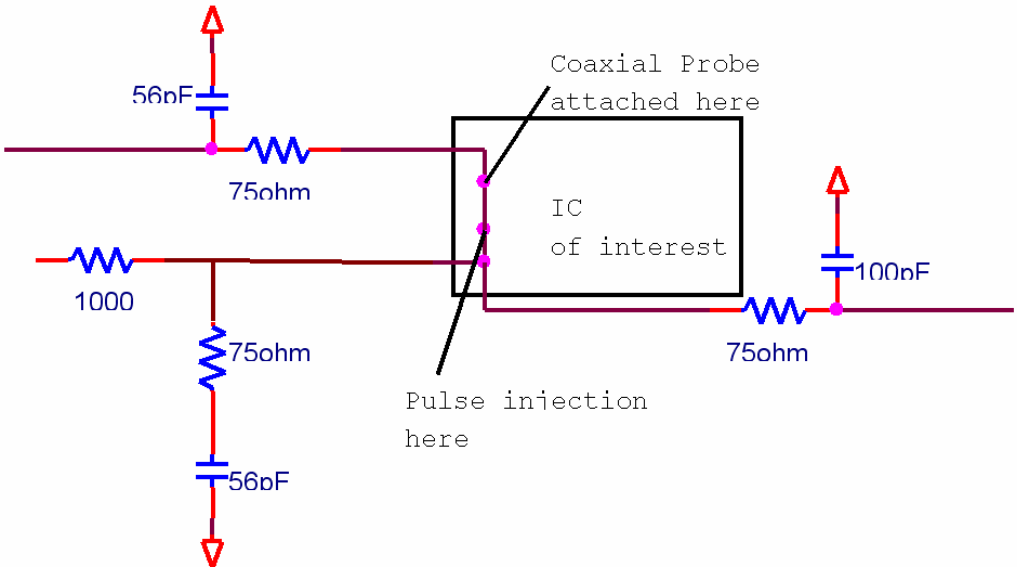

Fig. 15: *Circuit and added circuit elements to isolate the IC of interest from a widely distributed status line net.*

The IC of interest was part of a distributed net. To ensure that only the response of the IC of interest was measured all other ICs have been isolated by RC filters and the traces have been terminated to reduce reflects. A narrow pulse has been injected into the trace while observing the voltage at the IC of interest. The trace is normally logically high at about 1.3V, fig 16. The measured (ghazi oscilloscope, 50 cm coax connection) pulse only reduces the voltages to about 0.8 V. The pulse seen at the DIE might be somewhat different, partially as a result of the measurement frequency response and partially as a result of the interconnect inductance and input capacitance response.

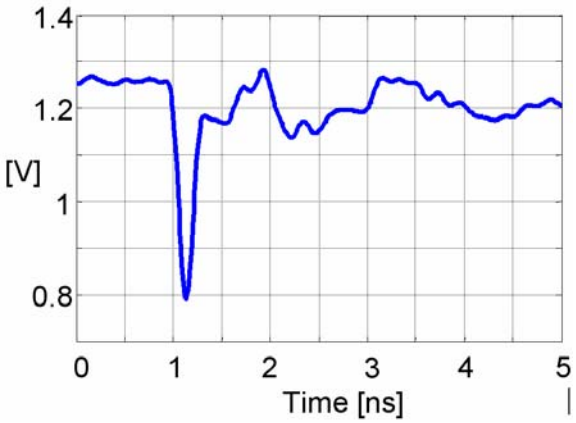

Fig. 16: *Measured voltage leading to a system crash.*

From a point of view of functionality, there is no need for the input to react that fast. Multiple on board (e.g., capacitor to ground or RC combination) and IC modification are possible to slow the response down to a level that ensures functionality, but reduces noise sensitivity.

Example case #2: Differential traces

Often people assume that a differential trace will offer good noise rejection due to its common mode rejection. This is true for many differential system, e.g., old analog telephone. But for fast digital systems this is often not the case, instead differential systems offer no better noise rejection then single-ended systems. Important aspects that determine the noise rejection of a digital system are:

- **Common mode range**. Many ICs have a relatively small common mode range, e.g., LVDS allows +/- 1V common mode. Any common mode larger than this might lead to a bit error. In most designs the common mode swing is no larger than 0V to VCC
- **Common mode termination.** While differential signals offer a good differential termination, there is often no termination for common mode waves. For example, on-chip differential termination by 100 Ohm will lead to an open circuit for a common mode signal. This will allow the common mode noise voltage to double, possibly driving the input into its common mode rail.
- **Common mode to differential mode conversion.** It is not easy to achieve more than 12 dB common to differential mode conversion, at frequencies > 1 GHz. In such a case a 2 V common mode signal would convert into a 500 mV differential signal. This is often larger than the nominal swing.

Susceptibility scanning showed a differential clock being very sensitive to ESD noise, fig 17.

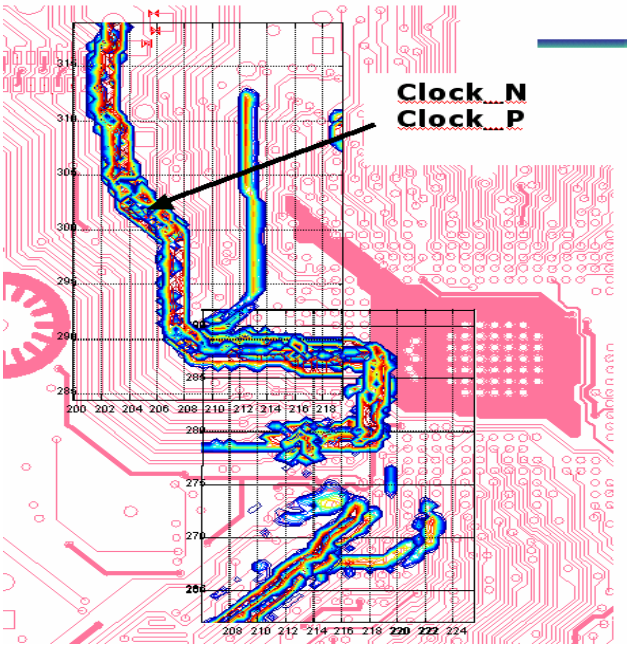

Fig. 17: *Scanning result on a prototype PCB. The Clock_N and Clock_P differential clock proved to be very noise sensitive.*

Response to differential mode noise

Probes have been attached to the trace (fig. 14) for capturing the noise voltages that lead to system upsets. As noise source narrow pulses have been injected in differential and in common mode. Expected as well as surprising results have been measured and verified on a second prototype board.

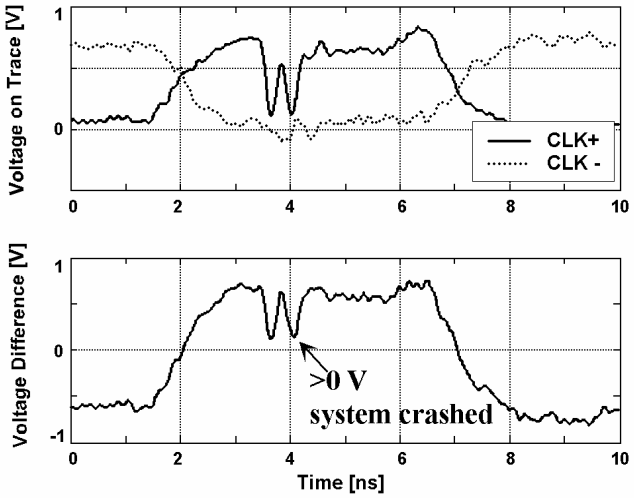

Figure 18: *Differential noise introduced into the clock. A negative pulse was added to CLK+. Although the difference (lower plot) does not reach 0V the system crashed.*

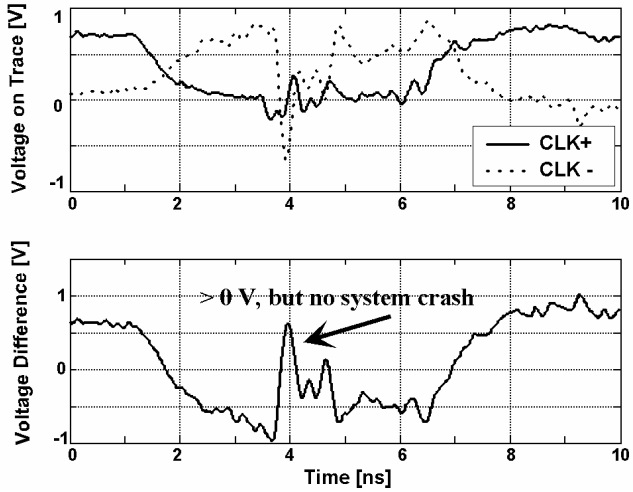

Figure 19: *Differential noise introduced on the clock. A negative pulse was introduced on CLK- The differential voltage was increased from -1V to about +0.5V, but no crash was observed for this type of events.*

The data shown in figs. 18 and 19 indicate that his specific input of the differential clock is not fully symmetric. It acts as if the threshold is at about 0.5V differential instead of being at 0V.

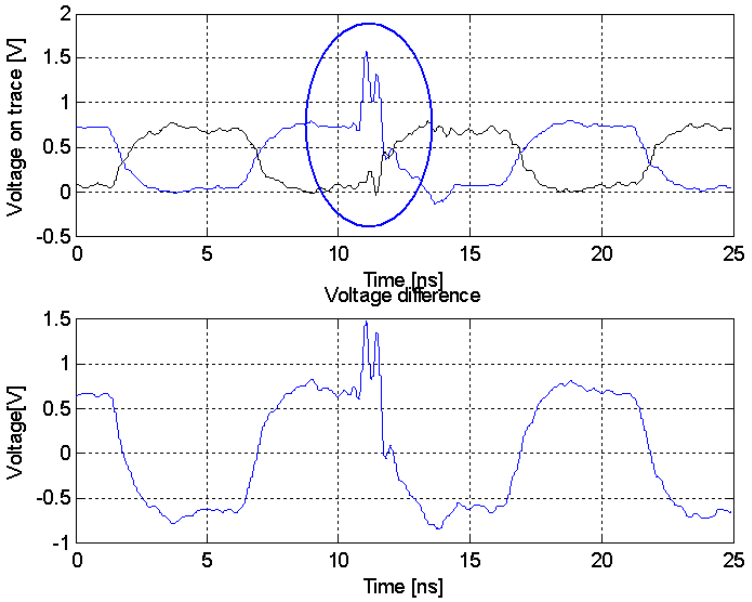

Fig. 20: Upset of a differential clock due to adding a positive pulse during a positive phase.

A couple of cases have been observed that indicate non-ideal response of the I/O buffers. An example is shown if fig. 20. A bit error is causing a system crash although a positive voltage is added to a differential signal in such a way that the noise increases the differential voltages without reaching ESD protection levels. Presently the reasons for such responses are under investigation using SPICE simulations.

Response to common mode noise

To inject common mode noise two 330 Ohm resistors have been connected to the traces and to the pulse generator. The noise level has been increased until upsets occurred.

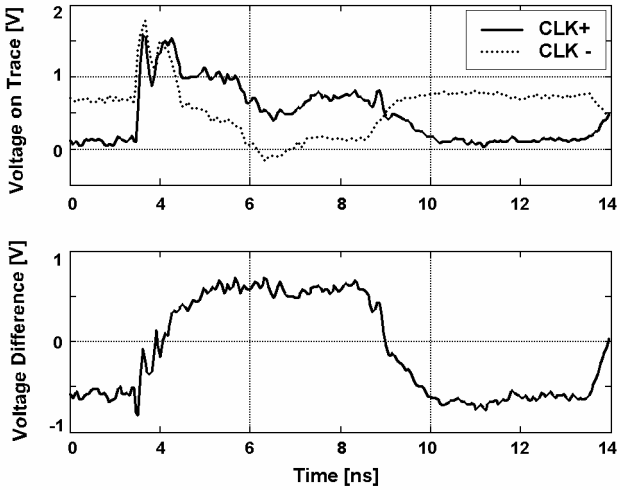

Figure 21: *Common mode noise introduced to a differential clock. This pulse is just underneath the level that would lead to a system upset. Note that the dotted line (top plot) nearly reaches the solid line indicating a clipping of the signal.*

The data shown in fig. 21 indicate that the common mode noise was correctly suppressed by the differential input. However a small increase of the common mode voltage beyond the values shown above will lead to system crash, fig. 22.

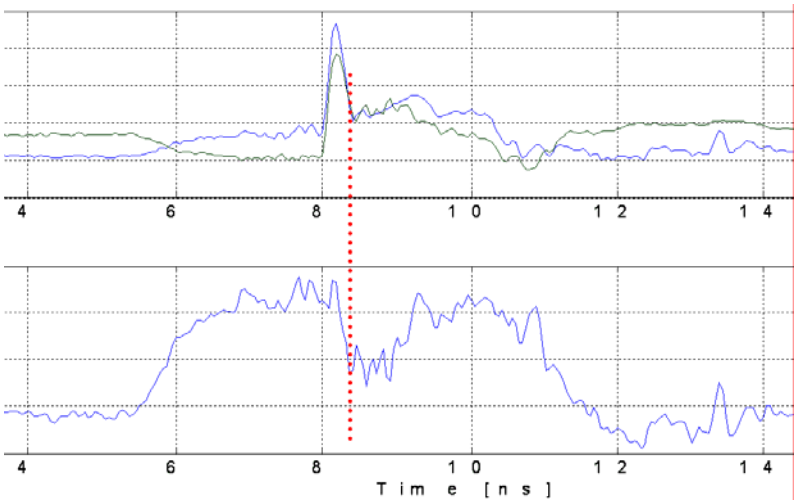

Fig. 22: *Common mode noise added to a differential trace. The difference (lower plot) maintains its correct value while the pulse is added (up to 8.3 ns, see the red line) but is disturbed thereafter. The differential voltage drops to about 0V leading to a system upset.*

The data above shows that only a few Volt of common mode will upset a differential system. A differential system may not more robust to common mode noise than a single ended (full swing) system. Design details matter: Is the system terminated for common mode? How strong is the CM to DM conversion? How large is the maximal CM swing under the worst case biasing condition? Of course, other arguments favor the differential system, but one should be careful in expecting any immunity improvement by switching to differential signaling. However, in EMI a large improvement is to be expected (as long as the drive is symmetric and the SSN current of the driver does not cause its own EMI problem) as the currents are much smaller and the symmetry will provide an additional 10 dB or more suppression.

Open questions

Years of reported effort in ESD robust design [14] together with improved PCB techniques (years ago most boars where 2 layers!), and denser design have provided many tools to engineers for reducing the number of ESD problems. On the other voltage swings have been reduced and more fast ICs are used in unshielded products. Overall, we believe that the number of ESD problems has gone down, but the difficulty in finding ESD problems has increased.

Near field scanning techniques, either done by hand or automatically, clearly help locating a certain class of ESD related problems. We see near field susceptibility scanning as the #1 tool for locating ESD upset problems, providing two main requirements are met:

- A waveform is used that is realistic for the type of problem one is after
- The number of pulses, possibly its timing and the EUT based software work together for detecting upsets with high probability.

However, a larger set of problems remains and might be a good focus of further investigation:

- **Immunity problems caused by global coupling**. Some of the upsets are not reproducible by local injection. We believe they are caused by global coupling to a board or are driven by “voltage” differences between boards. Other injection techniques are required for reliably causing them.
- **Correlation system level – board level.** The scanning provides board or IC level immunity information. But the most sensitive nets may not be the ones that cause a system level problem. The opposite is quite plausible: A very short, but highly sensitive trace will not form a good antenna while a much less sensitive trace that is routed via connectors will form a good antenna and is more likely to cause a system level problem. Further research needs to close the gap between system level and board and IC level.
- **IC level immunity test methods and robustness guidelines.** Most engineers like to avoid the detailed analysis of ESD, they need design guidelines for avoiding ESD problems. Filtering on PCB level may be too costly and, at present, it is difficult to predict when filtering is needed during the design phase. Test methods need to be developed that allow to quantify the soft-error sensitivity of ICs. Knowing such values and combining them with induced voltage levels one can estimate the risk of ESD disturbances. It should be possible to obtain induced voltage levels by using measured or simulated transfer functions between the ESD generator and the current and charge density on the board. Knowing the current and charge density one can define an “efficient loop area” of traces and interconnects to estimate the induced voltage or calculate the coupling more precise, or more elaborated directly from the field.
- **IC level immunity standards.** A variety of standards is being proposed, developed and drafted. Please check the developing IEC 62132 standards and related papers for further detail. Once established the standards will help IC designers to meet immunity targets and they will provide designers a known worst case sensitivity of selected ICs.
- **Software for improving immunity.** Software has been used for improving immunity for years. However, the increased use of FPGA might broaden the use. It is known that the placement of logic within and IC changes the EMI coupling from the IC to the board. Similar results are to be expected for immunity. Further, digital filtering techniques can be used to define the input response speed for lines that do not need to operate at the maximal FPGA speed.
- **Latch-up and ESD protection circuit recovery.** An interruption of logical functions can be caused by latch-up without leading to damage. This and possible effects of recovery in ESD protection circuits pose two possible paths for noise to cause upsets. How often they occur and which techniques increase or diminish these risks is not known as of now.

Conclusion

A three dimensional ESD scan system is developed to test the ESD sensitivity for digital devices. ESD susceptibility maps of a fast CMOS EUT are recorded for different types of pulse excitations and coupling mechanisms. The coupled noise in ESD sensitive traces are measured when an ESD soft error event occurs. This allows the identification of sensitive nets and enables us to capture voltage waveforms at the input of ICs at levels leading to a logical error. This type of information is used to improve IC, PCB and system design.

Acknowledgements

This was supported by Intel. We are especially thankful to Andy Martwick at Intel and Wang Kai (now with Intel) who performed most of the initial design of the test system.

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