Susceptibility Scanning as a Failure Analysis Tool for System-Level Electrostatic Discharge (ESD) Problems

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***Abstract*—Susceptibility scanning is an increasingly adopted method for root cause analysis of system-level immunity sensitivities. It allows localizing affected nets and integrated circuits (ICs). Further, it can be used to compare the immunity of functionally identical or similar ICs or circuit boards. This paper explains the methodology as applied to electrostatic discharge and provides examples of scan maps and signals probed during immunity scanning. Limitations of present immunity analysis methods are discussed.**

***Index Terms*—Electrostatic discharges (ESDs), immunity, scanning, susceptibility.**

I. Introduction

NEAR-FIELD electromagnetic interference (EMI) scanning techniques have been used for analyzing the fields above integrated circuits (ICs). The collection of near-field measuring data [6] is motivated by the desire to predict or analyze the EMI from electronic systems or to reconstruct the currents that flow from the IC or through its lead frame. Using near-field probing—as an injection tool—is a direct extension of the near-field scanning emission measurements mentioned before. However, a set of important differences need to be considered to successfully apply near-field scanning as a tool for analyzing immunity. Three important challenges need to be understood: 1) The scanning system needs feedback from the equipment under test (EUT) to recognize if a malfunction or degradation has occurred. 2) EMI scanning measures the field strength at a given frequency. However, in immunity testing, a wide variety of different noise types can be introduced during the scanning; thus, the user needs to determine the most appropriate type of noise. 3) The relationship between the setting of the disturbance source strength and the noise caused during a system test is highly complex; thus, it is difficult, and sometimes impossible, to directly relate system-level test results to local scanning results.

To avoid damage during testing, susceptibility scanning concentrates on analyzing soft errors, such as upsets, unwanted resets, or performance degradation. Although possible, it is less suitable for detecting destructive failures as the EUT would be lost on the first occurrence of a sensitive location. This paper addresses soft errors caused by electrostatic discharge (ESD)-like noise.

Different groups have used susceptibility scanning for analyzing ICs and printed circuit boards (PCBs). The common objective is identifying sensitive nets on circuits and direct coupling into the interconnect structures of ICs [1]–[6]. Such scanning can be done either as an initial step for implementing countermeasures or for quality inspection of functionally similar systems or ICs.

Once sensitive nets are identified, additional methods can be used to quantify the response of the circuit to electromagnetic disturbances. These methods are as follows:

1) direct injection to quantify the sensitivity of individual traces;
2) voltage probing on traces for analyzing the IC reaction to noise;
3) analysis of scan histograms; the histogram shows the number of occurrences of failures expressed in voltage levels allowing to compare systems statistically and to build knowledge bases for typical system performance.

The paper explains how the scanning method is applied for identifying sensitive nets, improving PCBs, and capturing signals on traces that help to analyze the IC response.

In Section II, we explain the scanning method used. Section III shows resulting scan maps, direct injection results, and voltages captured on traces during immunity testing. The limits of present implementations of immunity scanning are discussed in Section IV.

II. Experimental Method

Near-field scanning for immunity has been used by a variety of research groups [1]–[7]. The near-field scanning system is shown in Fig. 1. It follows the methodology described in [1] and [2].

The probe is moved to a predefined location using an *XYZ* and ϕ-motion system. It injects pulses that are either created in a transmission line pulser [8], [9] via the electric (E) or magnetic (M) field or using direct injection. The response of the EUT is observed. If a malfunction, such as a reset, loss of communication, or optical disturbance is detected, the EUT is reset and the point is retested starting from a lower test level.

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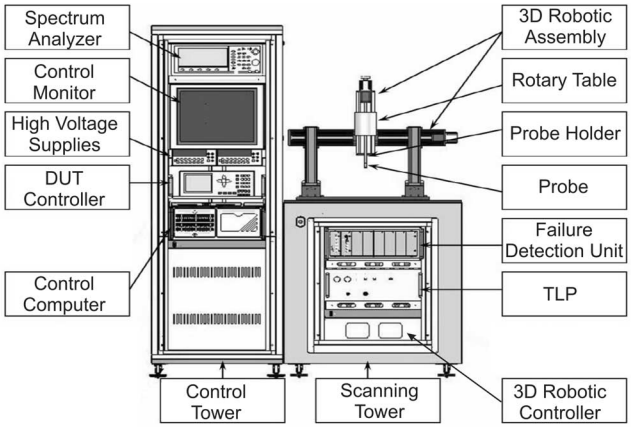

Fig. 1. Main components of the immunity scanning system.

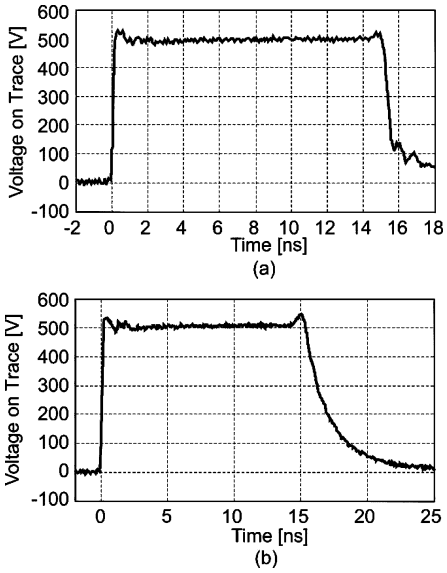

Fig. 2. Measured TLP output waveform at 500 V into a 50-Ω load. (a) Both edges of the pulse had the same voltage-derivative magnitude. (b) Slow falling edge.

The test level is increased until a malfunction is observed or the maximum test strength is reached; thereafter the next point is tested.

The software interface for monitoring the EUT allows flexibility for interfacing with different EUTs. In addition to analog and digital inputs, the interface can detect local area network violations and optical disturbances in screens.

In most cases, a transmission line pulser (TLP) is used as a disturbance source. The TLP can provide square-wave pulses up to 2500 V into a 50-Ω load. The rise time is less than 250 ps for charging voltages up to 5000 V (2500 V into a 50-Ω load). Depending on the application, high-voltage filters can be used for pulse shaping or transformer arrangements that allow increasing the pulse voltage. The rise time shown in Fig. 2 is less than 250 ps. A basic TLP provides a square-wave pulse. The falling edge of the pulse has been slowed down by a reverberation chamber (RC) combination that acts as a reverse termination. This allows distinguishing between effects caused

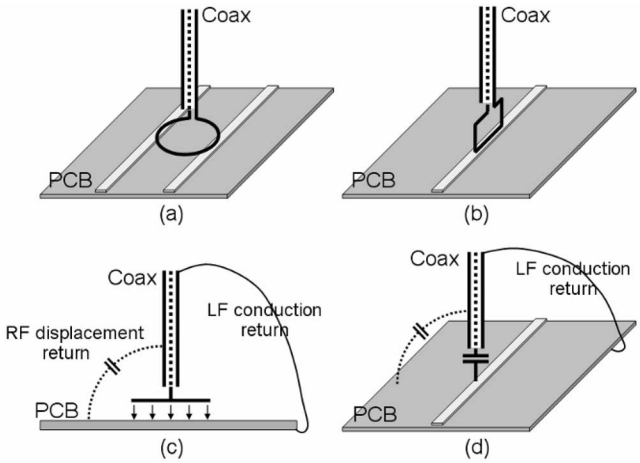

Fig. 3. Four different injection methods using various probes. (a) Horizontal loop probe. (b) Vertical loop probe. (c) E-field probe. (d) Direct capacitive injection probe.

by different polarities of the induced voltage. If both edges of the pulse had the same voltage derivative magnitude, then two pulses of equal amplitude but having opposite polarity would be injected into the circuit separated only by a few nanoseconds. Thus, it would be impossible to distinguish failures caused by the positive pulse from failures caused by the negative pulse. The slow falling edge forces the main noise induction to take place during the initial rise.

Since the circuit reaction is strongly determined by the wave impedance of the incident field, one needs to test for both *E*- and *H*-field coupling. For example, an input that is connected to a 10-kΩ pull-up will be sensitive to the *E*-field. Further, it was observed that most liquid crystal displays (LCDs) react predominately to the fast changing *E*-field. In contrast, if an input is connected via a 20-mm trace to a capacitor-to-ground, the trace will not react to the *E*-field, as the capacitor effectively grounds the trace. However, if a magnetic loop induces a series voltage between the input and the capacitor, the IC will react to the induced voltage. Consequently, there are four different injection methods, as shown in Fig. 3 [10]–[13].

The horizontal loop probe is a small loop attached to a semi-rigid coax. It induces a differential voltage if placed above a differential pair.

The magnetic field generated by the vertical loop probe induces voltages on the specific trace. For the 1 mm × 1 mm square-loop probe, the mutual inductance to a 0.18-mm-wide 50-Ω trace is about 0.4 nH. Thus, for a TLP setting of 1000 V, a pulse of 2 V is induced on this trace having a full-width at half-maximum of 200 ps.

The *E*-field probe consists of a metal plate connected to the inner conductor of the coax. The circular disk *E*-field probe, whose diameter is 9 mm, injects a pulse of 120 mA on a 0.18-mm-wide 50-Ω trace for a TLP setting of 1000 V, having a full-width at half-maximum of 500 ps.

The direct capacitive injection probe injects currents into the trace. The probe shown in Fig. 10 injects a pulse of 45 mA into a 0.5-mm-wide 50-Ω trace, having a full-width at half-maximum of 750 ps. The RF return current paths for the *E*-field

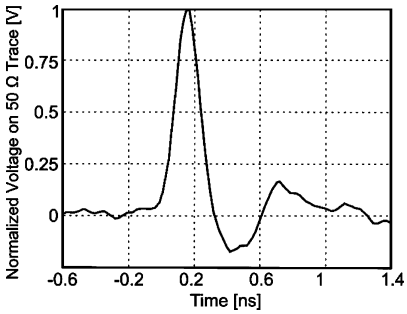

Fig. 4. Narrow pulse shape.

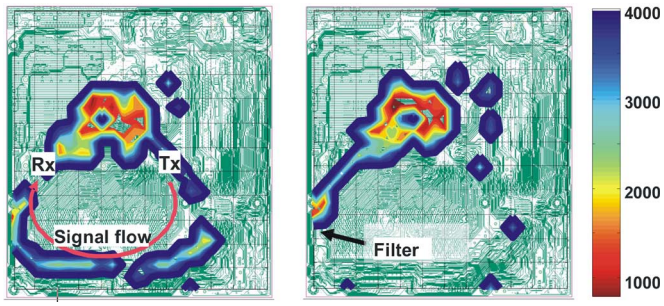

Fig. 5. ESD susceptibility map of a personal computer motherboard. (Left) Before filtering a sensitive trace. (Right) Rescan after inserting an RC filter into the trace. The color indicates the voltage setting at the TLP. A dark red color corresponds to 500 V, and a blue color corresponds to 4000 V. Areas that show no color could not be disturbed using voltages up to 5000 V. Scanning settings: horizontal *H*-field probe of 5 mm in diameter with a 3-mm step.

probe and direct capacitive injection probe are provided by the displacement current between the outer shield of the coax and the return (ground) plane of the circuit board. The LF current returns through the common ground conduction path.

It is difficult to determine the voltages or currents injected by *E*- or *H*-field probes *a priori*, as the coupling depends strongly on the local geometry. This problem can be circumvented by using direct capacitive injection. Due to the high impedance of the small capacitor, one can assume that the source impedance is much larger than the impedance formed by the trace, its driver, and the receiver. Thus, a known current is injected into the trace.

Several aspects need to be considered when selecting the right noise source. On one side, we want to induce voltages and currents that resemble the voltages and currents induced by the ESD. On the other side, the waveform should be as simple as possible. Two arguments assist us in selecting the waveform. First, the rising edge of the ESD causes the largest induced voltages, and second, experience has shown that most soft errors are hardly affected by the tail of the standardized ESD generator waveform [14], [15]. A transmission line pulse was selected as the pulse source for most investigations.

The ESD standard IEC 61000-4-2 calls for a 0.7–1-ns rise time. However, real ESD might show much shorter rise times [16], [17]. For selecting the correct pulse rise time, we must remind ourselves that the coupling between the field and a wire loop is proportional to the time derivative of the field. Thus, emphasis is given on the high-frequency content. It is reasonable to select a waveform that has a rise time shorter than the 0.7–1 ns given in the standard.

In experiments that analyze the reaction speed of IC inputs, we use the pulse shown in Figs. 2 and 4 having a full-width at half-maximum of about 200 ps.

The procedure to characterize the ESD susceptibility of an EUT was driven by a compromise between localization and test time.

1) *Initial coarse scan:* A scan is performed using a physically large probe (5 mm × 5 mm for the *H*-field probe) and a 4-mm step size. An initial ESD susceptibility map is generated showing sensitive areas.
2) *Fine scan:* Sensitive areas are analyzed using smaller probes and finer scan resolution.
3) *Trace voltage measurement:* The sensitive traces are analyzed and voltage measuring probes are attached to the trace to capture the voltages while injecting into the traces.
4) *Countermeasures:* After understanding the electrical function of the net, countermeasures can be designed.

The test time depends on: 1) the number of points; 2) the time needed to reboot a system; and 3) the duration during which ESD pulses are applied to each point. Commonly, pulses are applied at a rate of 20 Hz for 2 s. This leads to typical test times of 4 s per point, including time for positioning the probes.

After the initial coarse scan, a fine scan is performed, often using vertical H-field probes of 0.5 × 0.5 mm and 0.25 mm steps. This allows identifying individual traces on the board.

III. Measurement Results

In the following section, measurement results will be presented for illustrating different applications. The presentation follows the sequence that we apply in analyzing systems.

1) At first, a scan will provide an overview. This allows identifying sensitive traces for further probing. Next, individual traces are probed during injection to analyze the IC response.
2) Results for single-ended traces are shown.
3) Results for differential traces are shown.
4) The scanning is being used for comparing different designs of PCBs or ICs (*omitting in-depth analysis*).

A. Obtaining an Overview

The initial scan identifies sensitive regions. Reducing the probe size will allow identifying individual traces. Once sensitive traces are identified, countermeasures can be implemented. A typical result, contrasting before and after modifying a PCB, is shown in Fig. 5. A personal computer (PC) motherboard was scanned from the backside in Fig. 5 [18]. Less than ten nets were found to be sensitive. For such an EUT with only a few sensitive nets, it might be best to improve the PCB layout. Shielding would be a preferred alternative if many nets were found to be sensitive.

Fig. 5 shows the susceptibility of the backside of a PC motherboard. The sensitivity is dominated by a trace that originates close to the processor and terminates at the processor. However, due to suboptimal routing, it circles nearly half of the board,

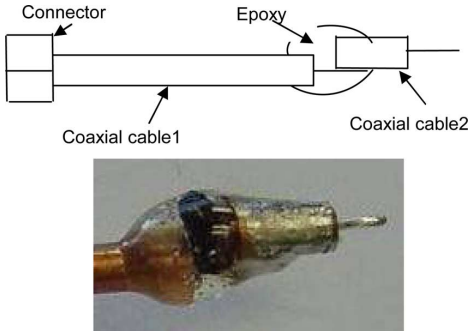

Fig. 6. Direct capacitive injection probe. The TLP pulse is injected through approximately 1 pF.

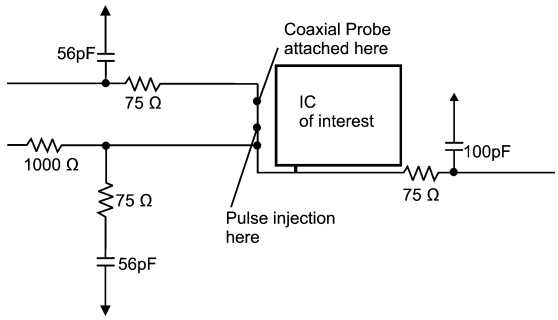

Fig. 7. Added RC circuit elements to isolate the IC of interest from a widely distributed status line net.

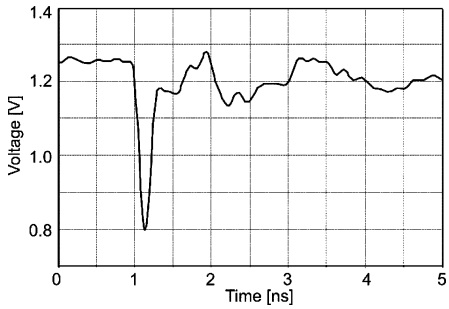

Fig. 8. Trace to ground voltage measured 10 mm from the IC. This impulse led to a system crash, but reducing the pulse by 10% did not lead to a system crash.

passes close to the edge, and close to the peripheral component interconnect (PCI) connector area. This region is usually an area of reduced shielding. The trace was filtered by an RC network. Thereafter, the board was rescanned to verify the improvement, as also shown in Fig. 5.

This example is typical for PCB layouts. While clock and data bus traces are routed very carefully for EMI and signal integrity reasons, there is less attention devoted to status lines. They may even connect boards through low-quality connectors or be routed close to the board edges. In this way, good antennas are formed. From an EMI emission perspective, it is only important that the status line carries a slow signal. However, from an immunity point of view, it is important how fast a trace can react to induced noise, no matter how slow (or low frequency) the intended signal is. Introducing the RC filter reduces the sensitivity of the net (Fig. 5) by filtering narrow pulses.

B. Single-Ended Trace Sensitivity

Scanning injects noise locally allowing to probe voltages and currents on affected nets and IC pins. This is a significant advantage over system-level testing. It is very difficult to perform voltage measurements during a system-level test, such as ESD applied during an IEC 61000-4-2 test. Most oscilloscope measurements will suffer from the very large common-mode currents induced during a system-level test. The localized nature of the scanning, especially the use of a magnetic loop that avoids inducing common-mode currents, might allow voltage measurements with a logic analyzer.

To capture the signal on a trace, the direct capacitive injection method is used. A capacitor is formed from a short piece of semirigid cable (see Fig. 6).

In a prototype system, it was observed that system-level ESD results were strongly dependent on the stepping level of one IC. The response of a specific status line was measured (see Fig. 7).

The IC of interest was part of the distributed net. To ensure that only the response of the IC of interest was measured, all other ICs were isolated by RC filters and the traces were terminated to reduce reflection. A narrow pulse was injected into the trace while observing the voltage at the IC of interest. The trace was normally at a logic high of about 1.3 V (see Fig. 8). During the ESD event, the voltage was briefly reduced to 0.8 V. The pulse seen at the die might be somewhat different, partially as a result of the measurement setup's frequency response and partially as a result of the interconnect inductance and IC input capacitance.

From the point of view of functionality, there is no need for the input to react that fast. The signal can be low-pass filtered to suppress narrow pulses. Different implementations of such a low-pass filter are possible, for example, onboard RC filters or digital filters within the IC.

C. Differential Trace Sensitivity

It is often assumed that a differential trace will offer good noise rejection due to its common-mode rejection. Certainly, this is true for well-implemented differential systems. An excellent example is an analog telephone. But, for fast digital systems, the implementation often overlooks design aspects. Consequently, differential systems might offer no better noise rejection than single-ended systems. Important aspects that determine the noise rejection of a digital system are as follows.

1) *Common-mode range:* Many ICs have a relatively small common-mode range, for example, low-voltage differential signaling (LVDS) allows ± 1 V common-mode. Any common-mode larger than this might lead to a bit error. In most designs, the common-mode swing is no larger than 0 V to common-collector voltage (VCC).
2) *Common-mode termination:* While differential signals provide a good differential termination, there is often no termination for common-mode waves. For example, on-chip differential termination by 100 Ω will lead to a nearly

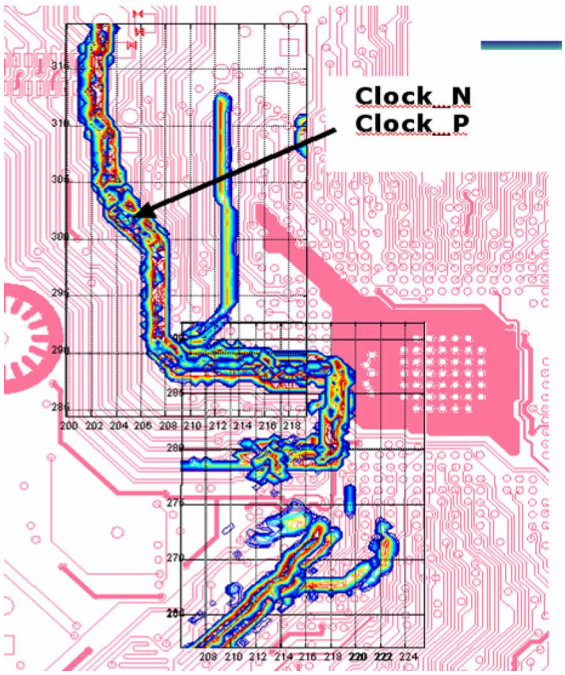

Fig. 9. Scanning result on a prototype PCB. The Clock_N and Clock_P of a differential clock proved to be very noise sensitive.

open circuit for a common-mode signal. This will allow the common-mode noise voltage to double, possibly driving the input into its common-mode rail.

3) *Common-mode to differential-mode conversion:* It may not be easy to achieve more than 12 dB of common-mode to differential-mode rejection at frequencies >1 GHz. In such a case, a 2-V common-mode signal would convert into a 500-mV differential signal. This is often larger than the nominal swing of the differential signal.

Susceptibility scanning showed a differential clock being very sensitive to ESD noise, as indicated in Fig. 9.

Probes have been attached to the trace to measure the noise voltages that lead to system upsets. Narrow pulses were injected as noise sources in both the differential and the common-mode. Some expected and some surprising results were observed and are presented next.

1) Response to Differential-Mode Noise: The data shown in Figs. 10 and 11 indicate that this differential clock input is not fully symmetrical. It acts as if the threshold is at about 0.5 V differential instead of 0 V.

A couple of cases were observed that indicate nonideal response of the I/O buffers. An example is shown in Fig. 12. A bit error caused a system crash although a positive voltage was added to a differential signal so that the noise increases the differential voltage without reaching ESD protection levels. Presently, the reasons for such responses are under investigation using simulation program with integrated circuit emphasis (SPICE) simulations.

2) Response to Common-Mode Noise: To inject common-mode noise, two 330-Ω resistors were connected to the traces and the pulse generator. The noise level was increased until

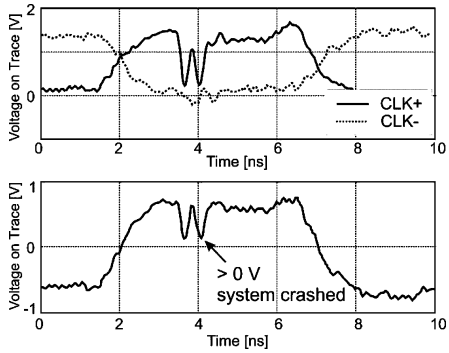

Fig. 10. Differential noise introduced into the clock. A negative pulse was added to CLK+. The system crashed even though the differential voltage (lower plot) did not reach 0 V.

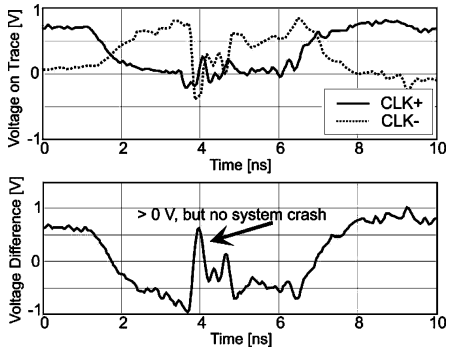

Fig. 11. Differential noise introduced on the clock. A negative pulse was introduced on CLK–. The differential voltage was increased from −1 V to about +0.5 V, but no crash was observed for this type of event.

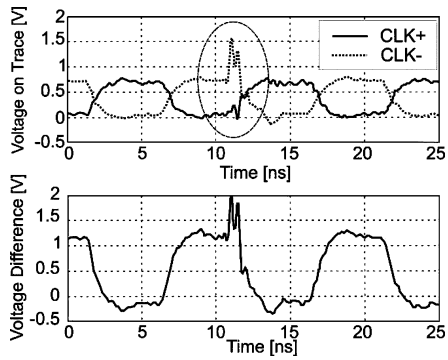

Fig. 12. Upset of a differential clock due to adding a positive pulse during a positive phase.

upsets occurred. Fig. 13 describes the common-mode noise injection method.

The data shown in Fig. 14 indicate that the common-mode noise was correctly suppressed by the differential input. However, a small increase of the common-mode voltage beyond the values shown before will lead to a system crash (Fig. 15).

The aforementioned data show that only a few volts of common mode will upset a differential system. A differential system may not be more robust to common-mode noise than a single-ended (full swing) system. Design details matter, such as the following.

1) Is the system terminated for common-mode?

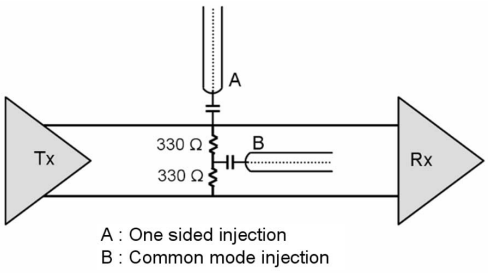

Fig. 13. Common-mode and one-sided noise injection.

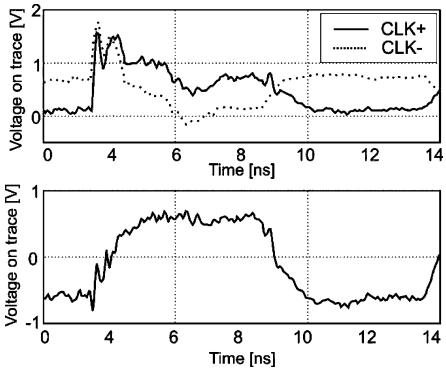

Fig. 14. Common-mode noise introduced to a differential clock. This pulse is just below the level that would lead to a system upset. Note that the dotted line (top plot) nearly reaches the solid line indicating a clipping of the signal.

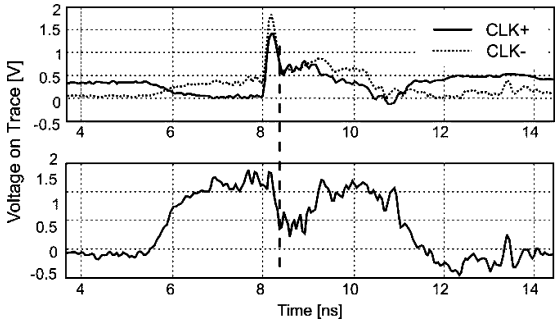

Fig. 15. Common-mode noise added to a differential trace. The difference (lower plot) maintains its correct value while the pulse is added (up to 8.3 ns, see the vertical dotted line) but is disturbed thereafter. The differential voltage drops to about 0 V leading to a system upset.

2) How strong is the common-mode to differential-mode conversion?
3) How large is the maximum common-mode swing under the worst case biasing condition?

1) Of course, other arguments favor the differential system, but one should be careful in expecting any immunity improvement by switching to differential signaling. However, in EMI, a large improvement can be expected (as long as the drive is symmetric and the simultaneous switching noise current of the driver does not cause its own EMI problem) as the currents are much smaller and the symmetry will provide an additional 10 dB or more suppression.

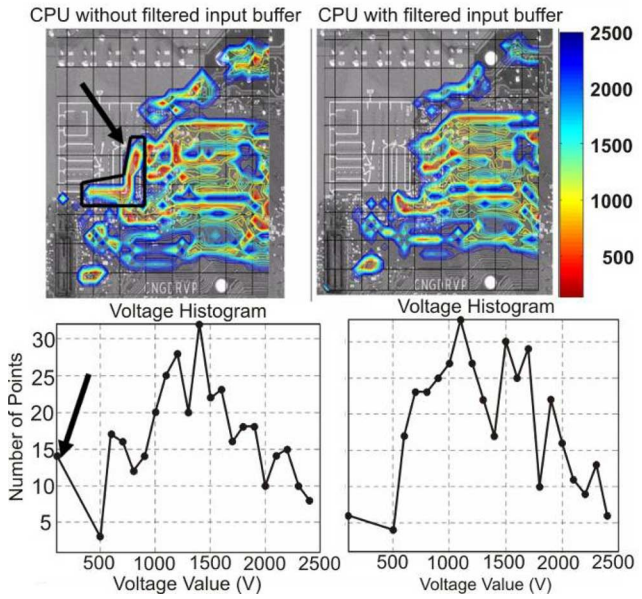

Fig. 16. Comparison of the scan maps on a PC motherboard for two different I/O buffer designs of a CPU. (Top) Scan map of a PC motherboard having prototype processors. The color grade indicates the voltage setting at the transmission line pulser. Red indicates sensitive areas. The most important difference is indicated by the arrow. An H-field probe of 5 mm $\times$ 5 mm and 1 mm step were used. (Bottom) Histogram showing the number of points experiencing a failure at a given level.

D. Comparing Functionally Identical ICs

Scanning can be used as a qualification tool, potentially allowing to omit a full system-level test if local scanning does not show an increased sensitivity to ESD. However, even small changes in an IC can worsen the ESD sensitivity. The consequence of a redesigned input buffer of a processor is shown in Fig. 16. The color scale indicates the voltage setting on the TLP. It is not obvious to scale the TLP setting to the voltage induced on a trace as such a scaling is dependent on the local geometry of the trace and the probe. However, the voltages on the trace can be measured, as shown in Section III of this paper. Important differences caused by the filtered input buffer are indicated in Fig. 16. The histograms are shown below the scan maps. The histograms indicate the number of occurrences of each failure level during scanning.

The most important difference between the left and the right data set is the reduction in very sensitive locations. The change in the input buffer reduced the number of test points that failed at 300 V from 14 to 6.

The scan maps shown in Fig. 17 compare two functionally identical ICs. The difference in sensitivity is large. Note that the sensitive region extends from the PCB through the bond wires onto the die. Thus, direct coupling into the IC is possible. This leaves the PCB designer little choice in improving the system-level performance.

Every time an IC manufacturing process is changed, its noise sensitivity can be affected. In the following example, a new process had been introduced. However, system-level testing using the new prototype showed reduced ESD robustness. As shown

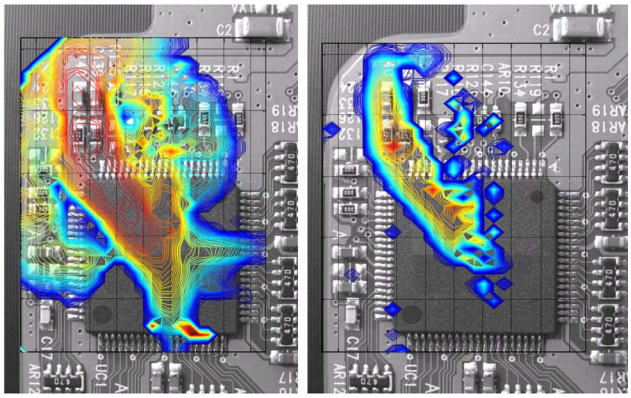

Fig. 17. Scan maps of two functionally identical but different ICs. The map combines by worst sensitivity four scanning results using a vertical H-field probe of 2 mm × 2 mm. For each scan, the probe is rotated by 90° to scan using both polarizations and polarities of the injected voltage. The step was 0.5 mm.

TABLE I
TRACE SENSITIVITY RESULTS FOR DIFFERENT INPUTS OF A STANDARD IC AND A PROTOTYPE IC

Pin Name	Mod B (new)	Mod A (old)
I	1000	> 4000
P	600	800
S	> 4000	> 4000
A	> 4000	> 4000
B	> 4000	> 4000
D	1000	> 4000

in Table I, the scanning revealed sensitive traces. The numbers indicate voltage settings at the TLP when the failure occurred. A 1 mm × 1 mm vertical *H*-field probe was used to compare the new prototype with a previous design. In both cases, the loop was positioned for maximum coupling into the trace.

ESD pulses can disturb displays. The disturbance can be brief, if, for example, a wrong synchronization pulse is created by the ESD, or it can be lasting if stored display settings are disturbed or if a power clamp is triggered and not able to recover. The scan results shown in Fig. 18 compare two display designs for the occurrence of brief disturbances caused by the ESD. They reveal sensitivities close to the gate and source drivers located on the edge of the glass. The ESD robustness differs significantly.

IV. DISCUSSION

We have observed that most system-level susceptibility is not caused by disturbances to clocks and busses but by disrupting status lines. Multiple reasons have been found.

1) Clock and bus traces are routed very carefully for EMI and signal integrity reasons.
2) Status lines often run over long distances. They pass from board to board and are often not treated with any filtering, since they do not cause any emission problems.
3) The input buffers are often too fast. Although the status line only changes rarely and often does not need to be synchronous to any clock event, it is received by input buffers that can react to less than 100-ps-wide pulses.

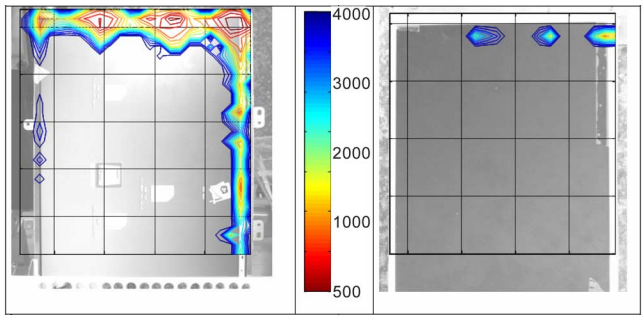

Fig. 18. Scan maps of two functionally identical displays created using a large horizontal *H*-field probe of 30 mm × 30 mm. The gate and source drivers of the LCD display are at the top and right, respectively. The color map corresponds to the voltage setting at the transmission line pulser.

The input buffers of ICs should be carefully selected to avoid unnecessary system sensitivity.

Near-field scanning methods are a developing tool for immunity analysis. So far, this method has provided excellent results if functionally identical parts are compared. However, right now, there are three test methods that have not been well linked:

1) system-level testing, e.g., IEC 61000-4-2, or -3, or –4;
2) PCB-level immunity scanning, as outlined in this paper;
3) IC direct susceptibility test methods (TEM cell, direct injection, etc.).

The link between methods needs further analysis. For example, for a given system-level test, how large will the surface field strengths be on a PCB? This is known for simplified structures via simulation, but in complex circuits, a mixture of deterministic and statistical methods might be needed to handle the variability of test points, gasket performance, and cable position.

On the other side, PCB scans discover sensitive nets well. But which nets form good antennas? Qualitatively, we know that traces that cross gaps, or attach to cables, or are close to the edge of the board form good antennas. But currently, there is no good method to quantify these antennas. Having such information available without a full EM simulation might allow a correlation between the system level and PCB level.

V. CONCLUSION

The paper has shown how near-field ESD scanning can be used for identifying sensitive nets, improving PCBs, and capturing the signals during immunity testing. It explains the probes used, the signals injected into traces, and the scanning and the probing methodology. Examples are given for the analysis of PCBs and for comparing functionally identical ICs. In its final part, it discusses the limits of scanning for immunity and briefly compares to system-level testing and other IC qualification methods.

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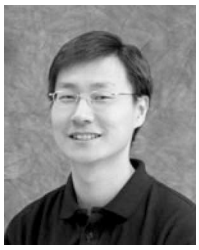

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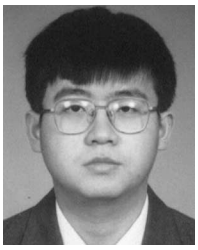

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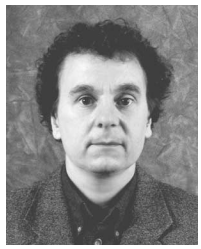

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